CALIBRATION AND SERVICING HANDBOOK

1062
1061A 1061

datron
INSTRUMENTS

digital voltmeter

CALIBRATION AND SERVICING HANDBOOK

for

THE DATRON AUTOCAL 1061 and 1061A DIGITAL VOLTMETERS

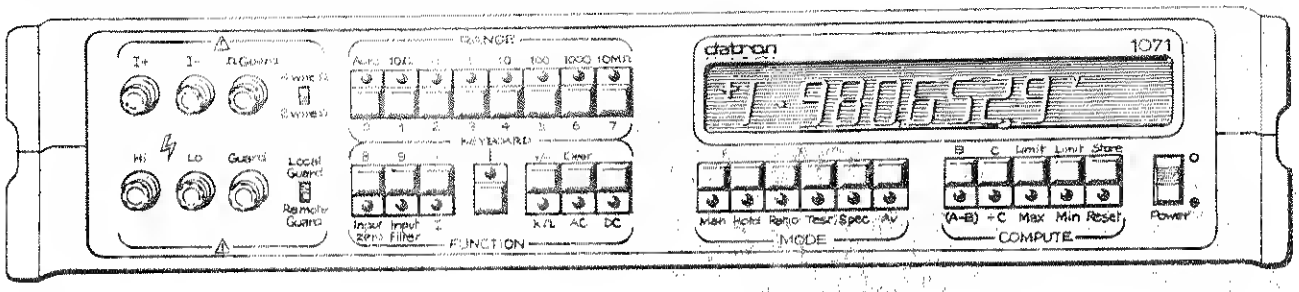
(for operating procedures
refer to the User's Handbook)

850045 Issue 9 (APRIL 1985)

For any assistance contact your nearest Datron Sales end Service center.
Addresses can be found at the back of this handbook.

Due to our policy of continuously updating our products, this handbook may contain minor differences in specification, components and circuit design to the instrument actually supplied. Amendment sheets precisely matched to your instrument serial number are available on request.

SECTION 1 THE 1061/1061A/1071 AUTOCAL INSTRUMENTS



The Datron 1061, 1061A and 1071 AUTOCAL multi-function, microprocessor controlled digital voltmeters (DVM) are high precision measuring instruments featuring exceptionally high stability and systems capability. The basic instrument provides full DC measurement capability, computation facilities, self check routines and calibration memory.

The AUTOCAL 1061 instrument combines high accuracy with short measurement time to maximize usability. A 5½ digit display provides a resolution of one microvolt and an accuracy of 5 ppm.

In the AUTOCAL 1061A, operation of the "Input Filter" key extends the display to 6½ digits to provide extra resolution to 100nV.
NB. Unless otherwise noted, references to "1061" in this Handbook apply also to 1061A instrument.

The AUTOCAL 1071 instrument maximizes accuracy with a 6½ digit display (7½, in the 'averaging' mode for 0.05 ppm resolution).

Standard and optional measurement facilities

In addition to the basic DC voltage measurement function, the instrument performance can be expanded, by the selection of options, to provide further measurements:

DC current
Resistance
True RMS AC voltage
True RMS AC current
DC coupled true RMS AC voltage
DC coupled true RMS AC current
Ratio

In addition, the standard 1061 and 1061A instruments provide a dB measurement.

The full range of options is as follows:

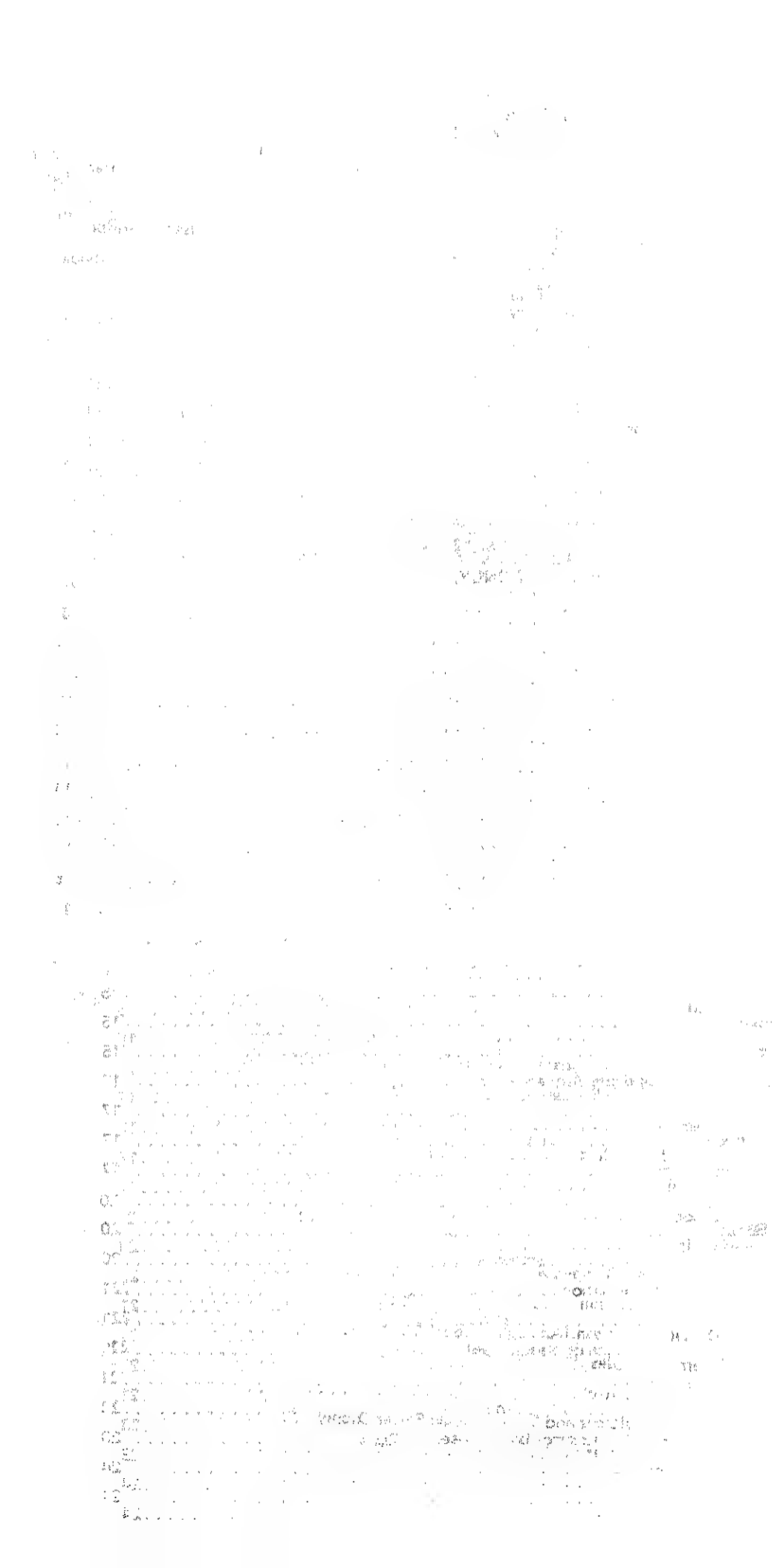
Option 10:	True RMS AC converter (DC plus 45Hz to 1MHz)
Option 12:	High Performance true RMS AC voltage converter (1061A only)
Option 20:	4-wire resistance measurement converter
Option 30:	DC and true RMS AC current converter (in conjunction with option 10 only)
Option 40:	Rear input / ratio input
Option 41:	Selectable rear input
Option 50:	IEEE 488 standard digital interface
Option 51:	BCD interface (1061 only)
Option 52:	External trigger
Option 70:	Analog output
Option 80:	115V 60Hz line operation
Option 81:	115V 50Hz line operation
Option 82:	115V 400Hz line operation
Option 90:	Rack mounting kit

Calibration

The AUTOCAL instruments have been designed to make the removal of the covers for calibration unnecessary, as full calibration of all ranges and functions can be carried out from the front panel.

The procedure for calibrating the instrument is contained in the Calibration and Servicing Handbook.

Accidental or unauthorised use of the calibration routine is prevented by a key operated switch on the instrument rear panel.



SECTION 1

CALIBRATION

1.1 INTRODUCTION

1.1.1 General

The purpose of calibration is to take account of any long-term drifts in the components of the instrument and to restore the accuracy, traceable to a known standard.

The period between calibrations depends upon the accuracy performance required from the instrument and for guidance, guaranteed accuracies for 24 hours, 90 days and 1 year are quoted.

The calibration procedures presented in the following pages should cater for most calibration situations. If, however, a special problem arises, please contact our Customer Service Section.

1.1.2 The Essentials for Good Calibration

Temperature - So that the instrument can meet its specification over the quoted temperature range, the temperature environment should be stabilised at 23°C ± 1°C. In addition, temperature gradients around the instrument should be considered, therefore calibrate the instrument in its normal operating position and allow plenty of room for ventilation.

Warm up - It is essential that the instrument has fully temperature stabilised if the best results from calibration are to be achieved. Therefore, at least a 2 hour warm-up period is recommended during which time the line supply or the covers should not be removed even for a short period. In addition, if the covers have been removed, make certain that they are correctly fitted and that the leaf contacts to the Earth and Guard Shields are in good shape.

Calibration Source - To perform a useful calibration the accuracy of the source should always be at least four times that of the instrument being calibrated. In most cases, examples of likely sources are given for each calibration function.

With some calibration sources, the output may take several seconds to settle to a final value, therefore unless a shorter settling time is assured, a period of 10 seconds is recommended before each calibration operation.

Guarding - It is preferable to arrange for the DVM to be calibrated with 'Local Guard' selected. Furthermore to arrange for the 'Lo' terminal of the DVM to remain at 'earth' throughout and let the calibration source float. If a 'Remote Guard' connection is necessary then examples are shown in the Operating Manual.

1.1.3 The 'AUTOCAL' Process

1.1.3.1 General

The Datron 'AUTOCAL' process means that complete calibration of AC, DC, Ohms and Current on every range can be carried out from the instruments own front panel. In the process, an internal non-volatile memory stores calibration constants for each function and range as determined when the instrument takes a series of 16 readings of the applied calibration source. Internally, each of the readings is deviated by one sixteenth of a digit and when an average is taken, the instrument is able to resolve to better than one least significant digit displayed.

Access to the non-volatile memory is gained using a key inserted into the rear panel. When calibration is complete, the key is removed, therefore preventing accidental or unauthorised use of the calibration routine.

1.1.3.2 Procedure Outline

- Select the 'FUNCTION' and 'RANGE' to be calibrated and cancel any 'MODE' or 'COMPUTE' buttons.

Insert the key into the 'CALIBRATE ENABLE' keyswitch on the rear panel and turn to the 'CAL' position. (The 'cal' legend will be displayed on the front panel.)

If the instrument is fitted with Option 50 IEEE Bus, set the rear panel address switch to 31 i.e. all 1's.

- Connect the calibration source to the input terminals and operate the keys shown in the tables in the following pages. When a 'CALIBRATE' button is operated, its associated L.E.D. indicator will light and extinguish when the calibration operation is executed.

- When all calibration is complete turn the keyswitch to 'RUN' and remove the key.

1.1.3.3 The Five 'AUTOCAL' Keys

'Zero' - This takes account of offsets in the instrument and in the calibration source.

'Gain' - This sets a scaling factor for each range and function.

'Ib' - This nulls the input bias current of the DC voltage measurement circuits to around 10pA. Therefore it only has a significant effect on the low DC voltage ranges and high resistance Ohms ranges. It can be operated as often as required and independently of other calibration operations. It will be seen that successive operations of 'Ib' approach the final nulled value of current iteratively.

'AcHf' - This flattens the response of the A.C. amplifier used for AC voltage measurement. It should only be used when a full calibration i.e. 'Zero', 'Gain' and 'AcHf' is carried out. As with 'Ib' the calibration action is iterative and requires several operations of the key to complete.

'Lin' - This is an important calibration operation as it optimises the basic linearity of the internal measurement circuitry used for all ranges and functions. It must be used before any DC voltage or Ohms calibration is carried out.

1.1.3.4 'AUTOCAL' using 'KEYBOARD'

This is an extension of the 'AUTOCAL' process which is useful when using a calibration source set to a nominal value but with known errors. This means for example that calibration directly to a standard cell is possible. A full explanation of the procedure is covered in section 1.7.

1.1.3.5 'AUTOCAL' over the Bus

Each of the five calibration operations can be controlled using Option 50, the IEEE bus. This means that the instrument can be entirely calibrated remotely or under program control. As mentioned in the 'Procedure Outline' for a manual calibration, the rear panel address switch should be set to 31, i.e. all 1's. When a bus calibration is required the address switch must be set to the address number assigned to the DVM in the system. More details of calibration with the bus are included in section 1.8.

1.1.3.6 'Error 4'

If during calibration 'Error 4' is displayed, this indicates that the Calibration Source deviates too far from the calibration span of the instrument. Under these circumstances, the calibration memory is not updated and the instrument goes into 'Hold' with the calibration button calibration key LED remains on.

In the case of 'Zero', 'Gain' or 'AcHf' the Calibration Source should be checked and the same 'CALIBRATE' key repressed. The 'Hold' mode may be released any time and the instrument will free run again. If 'Error 4' follows 'Ib' or 'Lin' or persistently appears following 'Zero', 'Gain' or 'AcHf' then an instrument failure may have occurred. Therefore either consult our Customer Service Section or the Servicing Section of this Handbook.

1.2 DC VOLTAGE CALIBRATION

1.2.1 General

The procedure in the table opposite is all that is necessary to completely 'AUTOCAL' the DC voltage function. Steps 1 and 2 affect the accuracy on all ranges and should therefore be carried out even if just one range is being calibrated.

On each range a 'Zero' and 'Gain' calibration is required for each polarity of input. The two 'Zero' calibrations are included to overcome a possible zero difference with the polarity setting of the DC calibration source.

If the 'DVM Reading After Calibration' is not in accordance with the table, repeat operations of the same 'CALIBRATE' key are permissible. Where no tolerance is shown in this column, only the exact reading quoted with an occasional least significant digit showing is to be expected.

1.2.2 Equipment Required

- 1MΩ 'Lin' Source. This is a 1MΩ 5% resistor in parallel with a 1nF capacitor, shielded to reduce noise interference.

- 10MΩ 'Ib' Source. This is a 10MΩ 5% resistor in parallel with a 1nF capacitor, shielded to reduce noise interference.

Datron products, number 400391 and 400392, are available as 'Lin' and 'Ib' sources and are recommended.

- A DC Calibration Source. e.g.: Datron 4000/4000A Autocal Standard.

1.2.3 Checking Accuracy after 'AUTOCAL'

To check the accuracy after 'AUTOCAL' the 'Specification Verification' section of the User's Handbook will be useful; it provides tables for quick reference of accuracy on all ranges and functions in displayed digits.

DC VOLTAGE CALIBRATION

Step	Calibration Operation	Calibration Source Output	DVM Setting	'CALIBRATE' Key	DVM Reading After Calibration	Remarks
1	Linearity	1MΩ Lin Source	DC,1 Filter[1]	'Lin'	<10 digits (<100 digits)	This calibration step may take around 30 seconds to complete
2	Input Bias Current	10MΩ Ib Source	DC,.1	'Ib'	<100 digits	Each subsequent operation of 'Ib' should approximately halve the DVM reading
3	10V Range Zero	+0.0000V	DC,10	'Zero'	±0.0000V	
4	10V Positive Full Range	+10.0000V	DC,10	'Gain'	+10.0000V	
5	10V Range Zero	−0.0000V	DC,10	'Zero'	±0.0000V	
6	10V Negative Full Range	−10.0000V	DC,10	'Gain'	−10.0000V	
7	1V Range Zero	+0.00000V	DC,1	'Zero'	±.00000V	
8	1V Positive Full Range	+1.00000V	DC,1	'Gain'	+1.00000V	
9	1V Range Zero	−0.00000V	DC,1	'Zero'	±.00000V	
10	1V Negative Full Range	−1.00000V	DC,1	'Gain'	−1.00000V	
11	.1V Range Zero	+0.000mV	DC,.1	'Zero'	±0.000mV ±1 digit	Wait for the reading to stabilize before operating 'Zero'
12	.1V Positive Full Range	+100.000mV	DC,.1	'Gain'	+100.000V ±1 digit	
13	.1V Range Zero	−0.000mV	DC,.1	'Zero'	±0.000mV ±1 digit	Wait for the reading to stabilize before operating 'Zero'
14	.1V Negative Full Range	−100.000mV	DC,.1	'Gain'	−100.000V ±1 digit	
15	100V Range Zero	+0.000V	DC,100	'Zero'	±0.000V	
16	100V Positive Full Range	+100.000V	DC,100	'Gain'	+100.000V	
17	100V Range Zero	−0.000V	DC,100	'Zero'	±0.000V	
18	100V Negative Full Range	−100.000V	DC,100	'Gain'	−100.000V	
19	1000V Range Zero	+0.00V	DC,1000	'Zero'	±0.00V	
20	1000V Positive Full Range	+1000.00V	DC,1000	'Gain'	+1000.00V	⚡ Lethal voltages present - increase calibration source in 100V steps if possible
21	1000V Range Zero	−0.00V	DC,1000	'Zero'	±0.00V	
22	1000V Negative Full Range	−1000.00V	DC,1000	'Gain'	−1000.00V	⚡ Lethal voltages present - increase calibration source in 100V steps if possible

[1] For 1061A, Input Filter increases resolution by 1 digit – 1061A tolerance given in brackets ( ).

1.3 OHMS CALIBRATION

1.3.1 General

The procedure in the table opposite is all that is necessary to completely 'AUTOCAL' the Ohms function. If just the Ohms or just one range of the Ohms is to be calibrated, then steps 1 and 2 in the DC Voltage Calibration table should be carried out first. Then on each Ohms range just a 'Zero' and 'Gain' calibration is required.

If the 'DVM Reading After Calibration' is not in accordance with the table, repeat operations of the same 'CALIBRATE' key is permissible to improve the reading. Where no tolerance is shown in this column, only the exact reading quoted with an occasional least significant digit showing is to be expected.

1.3.2 'Zero' Resistance Source

For accurate 'Zero' calibration on Ohms it is ESSENTIAL that a correctly connected zero source is used. Two arrangements are necessary as shown in Fig. 1.1; it can be seen that '4 wire Ω' selection is recommended on all ranges.

1.3.3 Equipment Required

A set of resistance standards from 10Ω to 10MΩ in decades; it is essential that 10Ω to 100kΩ standards are 4 terminal devices. e.g. Datron 4000/4000A Autocal Standard with Option 20.

1.3.4 Checking Accuracy after 'AUTOCAL'

To check the accuracy after 'AUTOCAL' the 'Specification Verification' section of the Operating Handbook will be useful. It provides tables for quick reference of accuracy on all ranges and functions in displayed digits.

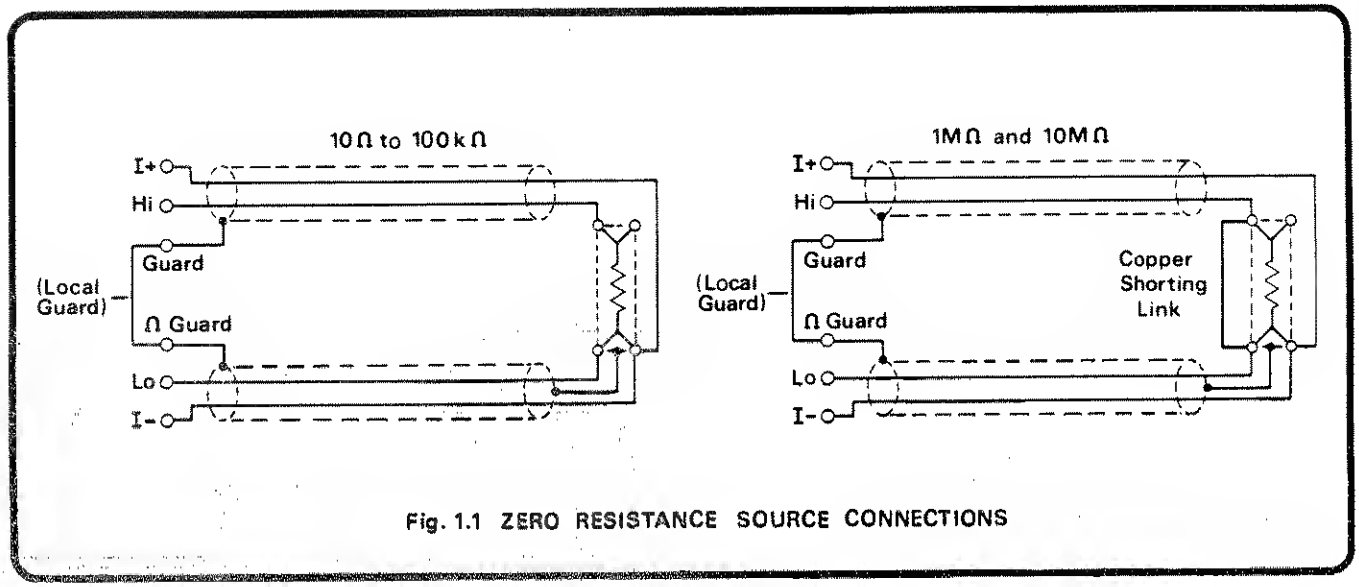


Fig. 1.1 ZERO RESISTANCE SOURCE CONNECTIONS

OHMS CALIBRATION TABLE

Step	Calibration Operation	Calibration Source	DVM Setting	'CALIBRATE' Key	DVM Reading After Calibration	Remarks
1	10Ω Range Zero	4 wire zero	kΩ, 4 wire, 10Ω	'Zero'	±0.0000Ω ±1 digit	Wait for the reading to stabilize before operating 'Zero'
2	10Ω Full Range	10Ω [1] Standard Resistor	kΩ, 4 wire, 10Ω	'Gain'	10.0000Ω ±1 digit	Wait for the reading to stabilize before operating 'Gain'
3	.1kΩ Range Zero	4 wire zero	kΩ, 4 wire, .1	'Zero'	±0.000Ω	
4	.1kΩ Full Range	100Ω [1] Standard Resistor	kΩ, 4 wire, .1	'Gain'	100.000Ω	
5	1kΩ Range Zero	4 wire zero	kΩ, 4 wire, 1	'Zero'	±.00000kΩ	
6	1kΩ Full Range	1kΩ [1] Standard Resistor	kΩ, 4 wire, 1	'Gain'	1.00000kΩ	
7	10kΩ Range Zero	4 wire zero	kΩ, 4 wire, 10	'Zero'	±0.0000kΩ	
8	10kΩ Full Range	10kΩ [1] Standard Resistor	kΩ, 4 wire, 10	'Gain'	10.0000kΩ	
9	100kΩ Range Zero	4 wire zero	kΩ, 4 wire, 100	'Zero'	±0.000kΩ	
10	100kΩ Full Range	100kΩ [1] Standard Resistor	kΩ, 4 wire, 100	'Gain'	100.000kΩ	
11	1000kΩ Range Zero	4 wire zero	kΩ, 4 wire, 1000 Input Filter[2]	'Zero'	±0.00kΩ (±0.000kΩ)	
12	1000kΩ Full Range	1000kΩ [1] Standard Resistor	kΩ, 4 wire, 1000 Input Filter[2]	'Gain'	1000.00kΩ ±1 digit (1000.000kΩ) (±10 digits)	
13	10MΩ Range Zero	4 wire zero	kΩ, 4 wire, 10MΩ Input Filter[2]	'Zero'	±0.0000MΩ (±0.00000MΩ)	
14	10MΩ Full Range	10MΩ [1] Standard Resistor	kΩ, 4 wire, 10MΩ Input Filter[2]	'Gain'	10.0000MΩ ±5 digits (10.00000MΩ) (±50 digits)	

[1] - With Standard Resistor sources it may be useful to use the 'KEYBOARD' method of calibration - see section 1.7

[2] - For 1061A, Input filter increases resolution by 1 digit, so 1061A figures are given in brackets ( ).

1.4 AC VOLTAGE CALIBRATION – OPTION 10 ONLY

1.4.1 General

The procedure in the table opposite is all that is necessary to completely 'AUTOCAL' the AC voltage function. On each range just a 'Zero', 'Gain' and 'AcHf' calibration is required.

If the 'DVM Reading After Calibration' is not in accordance with the table, repeat operation of the same 'CALIBRATE' key is permissible to improve the readings. This will be necessary with the AcHf key.

1.4.2 Equipment Required

A copper shorting link and an AC calibration source e.g. Datron 4200 Autocal AC Standard.

1.4.3 Checking Accuracy after 'AUTOCAL'

To check the accuracy after 'AUTOCAL' the 'Specification Verification' section of the Operating Handbook will be useful. It provides tables for quick reference of accuracy on all ranges and functions in displayed digits.

AC VOLTAGE CALIBRATION TABLE (OPTION 10 ONLY)

Step	Calibration Operation	Calibration Source Output	DVM Setting	'CALIBRATE' Key	DVM Reading After Calibration	Remarks
1	DC coupled AC Zero	Copper Shorting link	AC,DC,.1	'Zero'	0.000mV ±3 digits	Set 'Local Guard'. Do not set 'Input filter'. Wait for reading to stabilize before operating 'Zero'
2	.1V Range Zero	Copper Shorting link	AC,.1	Check only	<100 digits	
3	1V Range Zero	Copper Shorting link	AC,1	'Zero'	.00000V ±1 digit	
4	10V Range Zero	Copper Shorting link	AC,10	'Zero'	0.0000V ±1 digit	
5	100V Range Zero	Copper Shorting link	AC,100	'Zero'	0.000V ±1 digit	
6	1000V Range Zero	Copper Shorting link	AC,1000	'Zero'	0.00V ±1 digit	
7	10V Full Range LF	10V rms 500 Hz	AC,10 Input Filter	'Gain'	10.0000V ±1 digit	Select 'Input filter' for remaining steps
8	10V Full Range HF	10V rms 30 kHz	AC, 10 Input filter	'AcHf'	10.0000V ±5 digits	
9	1V Full Range LF	1V rms 500Hz	AC,1 Input filter	'Gain'	1.00000V ±1 digit	
10	1V Full Range HF	1V rms 30 kHz	AC,1 Input filter	'AcHf'	1.00000V ±5 digits	
11	.1V Full Range LF	.1V rms 500 Hz	AC,.1 Input filter	'Gain'	100.000mV ±2 digits	
12	.1V Full Range HF	.1V rms 30 kHz	AC,.1 Input filter	'AcHf'	100.000mV ±5 digits	
13	100V Full Range LF	100V rms 500 Hz	AC,100 Input filter	'Gain'	100.000V ±1 digit	
14	100V Full Range HF	100V rms 30 kHz	AC,100 Input filter	'AcHf'	100.000V ±5 digits	
15	1000V Full Range LF	1000V rms 500 Hz	AC,1000 Input filter	'Gain'	1000.00V ±1 digit	↯ Lethal voltage present. - increase calibration source in 100V steps if possible
16	1000V Full Range HF	1000V rms 20kHz	AC,1000 Input filter	'AcHf'	1000.00V ±5 digits	↯ Lethal voltage present - increase calibration source in 100V steps if possible. DO NOT EXCEED 25 kHz

1.4 AC VOLTAGE CALIBRATION – 1061A OPTION 12 ONLY

1.4.4 General

The procedure in the table opposite is all thet is necessary to completely 'AUTOCAL' the AC voltage function. On eech renge just a 'Zero', 'Gain' and 'AcHf' calibretion is required.

If the 'DVM Reading After Calibration' is not in accordance with the table, repeet operation of the same 'CALIBRATE' key is permissible to improve the readings. This will be necessary with the AcHf key.

Note: To reduce the effect of noise at low input levels, AC zero calibration is carried out at 0.1% Range; and for 100mV Range zero (steps 1 & 2 of the table), Guard is connected to Lo using a copper shorting link.

1.4.5 Equipment Required

A copper shorting link and en AC calibration source e.g. Detron 4200 Autocal AC Standard.

1.4.6 Checking Accuracy after 'AUTOCAL'

To check the accuracy after 'AUTOCAL' the 'Specification Verification' section of the User's Handbook can be employed. It describes the use of 'Spec' mode to verify the accuracy of the instrument, also providing a report sheet 'master copy' for compilation of permanent records.

AC VOLTAGE CALIBRATION TABLE (1061A OPTION 12 ONLY)

Step	Calibration Operation	Calibration Source Output	DVM Setting	'CALIBRATE' Key	DVM Reading After Calibration	Remarks
1	DC coupled AC Zero	0.100mV 500Hz (short Guard to Lo)	AC,DC,.1	'Zero'	0.100mV ±10 digits	Set 'Local Guard'. Do not set filter in. Wait for reading to stabilize before operating 'Zero'
2	.1V Range Zero	Short Hi to Lo to Guard	AC,.1	Check only	< 100 digits	
3	1V Range Zero	0.00100V 500Hz	AC,1	'Zero'	0.00100V ±1 digit	
4	10V Range Zero	0.0100V 500Hz	AC,10	'Zero'	0.010,0V ±1 digit	
5	100V Range Zero	0.100V 500Hz	AC,100	'Zero'	0.100V ±1 digit	
6	1000V Range Zero	1.00V 500Hz	AC,1000	'Zero'	1.00V ±1 digit	
7	10V Full Range LF	10V rms 500Hz	AC,10	'Gain'	10.000,0V ±1 digit	
8	10V Full Range HF	10V rms 30KHz	AC,10	'AcHf'	10.000,0V ±10 digits	
9	1V Full Range LF	1V rms 500Hz	AC,1	'Gain'	1.000,00V ±1 digit	
10	1V Full Range HF	1V rms 30kHz	AC,1	'AcHf'	1.000,00V ±10 digits	
11	.1V Full Range LF	.1V rms 500Hz	AC,.1	'Gain'	100.000mV ±2 digits	
12	.1V Full Range HF	.1V rms 30kHz	AC,.1	'AcHf'	100.000mV ±10 digits	
13	100V Full Range LF	100V rms 500Hz	AC,100	'Gain'	100.000V ±1 digit	
14	100V Full Range HF	100V rms 30kHz	AC,100	'AcHf'	100.000V ±10 digits	
15	1000V LF Range Gain	500V rms 500Hz	AC,1000	'KEYBOARD 500V' 'Gain'	500.00V ±1 digit	Lethal voltage present - increase calibration source in 100v steps if possible
16	1000V HF Range Gain	500V rms 20kHz	AC,1000	'KEYBOARD 500V' 'AcHf'	500.00V ±15 digits	Lethal voltage present - increase calibration source in 100V steps if possible. DO NOT EXCEED 25kHz

1.5 DC CURRENT CALIBRATION

(No DC Current facility if Option 12 is fitted)

1.5.1 General

The procedure in the table below shows all that is necessary to completely 'AUTOCAL' the DC Current function. If just the DC Current or just one range of DC Currant is to be calibrated, then step 11 to 14 of the DC Voltage Calibration table should be carried out first. Then on each DC Current ranga just a 'Zero' and 'Gain' calibration is required.

If tha 'DVM Reading After Calibration' is not in accordance with the table then repeat operation of the same 'CALIBRATE' key is permissible to improve the reading. Where no tolerance is shown in this column, only the exact reading quoted with an occasional least significant digit showing is to be expected.

1.5.2 Equipment Required

A DC Current calibration source. e.g. Datron 4000/4000A Autocal Standard with Option 20.

1.5.3 Checking Accuracy after 'AUTOCAL'

To check the accuracy after 'AUTOCAL' the 'Specification Verification' section of the Operating Handbook will be useful. It provides tables for quick reference of accuracy on all ranges and functions in displayed digits.

DC CURRENT CALIBRATION TABLE

Step	Calibration Operation	Calibration Source Output	DVM Satting	'CALIBRATE' Key	DVM Reading After Calibration	Remarks
1	.1mA Range Zero	0.000μA	DC,I,.1	'Zero'	±0.000μA ±1 digit	Do not select 'Input filter'
2	.1mA Full Range	+100.000μA	DC,I,.1	'Gain'	+100.000μA ±2 digits	
3	1mA Range Zero	0.00000mA	DC,I,1	'Zero'	±.00000mA ±1 digit	
4	1mA Full Range	+1.00000mA	DC,I,1	'Gain'	+1.00000mA ±2 digits	
5	10mA Range Zero	0.0000mA	DC,I,10	'Zero'	±0.0000mA ±1 digit	
6	10mA Full Range	+10.0000mA	DC,I,10	'Gain'	+10.0000mA	
7	100mA Range Zero	0.000mA	DC,I,100	'Zero'	±0.000mA	
8	100mA Full Range	+100.000mA	DC,I,100	'Gain'	+100.000mA	
9	1000mA Range Zero	0.00mA	DC,I,1000	'Zero'	±0.00mA	
10	1000mA Full Range	+1000.00mA	DC,I,1000	'Gain'	+1000.00mA	

1.6 AC CURRENT CALIBRATION

(In conjunction with Option 10 only)

1.6.1 General

The procedure in the table below shows all that is required to completely 'AUTOCAL' the AC Current function. If just the AC Current or just one range of AC Current is to be calibrated, then steps 1, 2, 11 & 12 of the Dption 10 AC Voltage Calibration table must be carried out first. Then on each range just a 'Zero' and 'Gain' calibration is required.

If the 'DVM Readlng After Calibration' is not in accordance with the table then repeat operations of the same 'CALIBRATE' key is permissible to improve the reading.

1.6.2 Equipment Required

An AC Current calibration source at 1kHz. e.g. Datron 4200 Autocal AC Standard with option 30.

1.6.3 Checking Accuracy after 'AUTDCAL'

To check the accuracy after 'AUTOCAL' the specification Verification section of the Operation Handbook will be useful. It provides tables for quick reference of accuracy on all ranges and functions in displayed digits.

AC CURRENT CALIBRATIDN TABLE

Step	Calibration Operation	Calibration Source Dutput	DVM Setting	'CALIBRATE' Key	DVM Reading After Calibration	Remarks
1	DC coupled AC Zero	No connections to DVM input terminals	I,DC,AC,.1	'Zero'	0.000μA ±5 digits	Do not select 'Input filter'
2	.1mA Range Zero	"	I,AC,.1	Check only	<±100 digits	Cancel DC coupled
3	1mA Range Zero	"	I,DC,AC,1	'Zero'	.00000mA ±5 digits	
4	10mA Range Zero	"	I,DC,AC,10	'Zero'	0.0000mA ±5 digits	
5	100mA Range Zero	"	I,DC,AC,100	'Zero'	0.000mA ±5 digits	
6	1000mA Range Zero	"	I,DC,AC,1000	'Zero'	0.00mA ±5 diglts	
7	.1mA Full Range	100μA, 1kHz	I,DC,AC,.1	'Gain'	100.000μA ±10 diglts	
8	1mA Full Range	1mA, 1 kHz	I,DC,AC,1	'Gain'	1.00000mA ±10 digits	
9	10mA Full Range	10mA, 1 kHz	I,DC,AC,10	'Gain'	10,0000mA ±10 digits	
10	100mA Full Range	100mA, 1 kHz	I,DC,AC,100	'Gain'	100,000mA ±10 digits	
11	1000mA Full Range	1A, 1 kHz	I,DC,AC,1000	'Gain'	1000.00mA ±10 digits	

1.7 CALIBRATION USING 'KEYBOARD'

1.7.1 General

The 'KEYBOARD' method of calibration is useful when a calibration source although set to a nominal value has known errors. In this situation the known value of the calibration source can be entered into the DVM before the 'AUTOCAL' process is executed. The process is functional during any calibration with a source of magnitude between 20% and 200% of the range selected, but it should be noted that for equal magnitude source errors, calibrating at the lower percentage end of range produces a higher percentage calibration error. The 'KEYBOARD' method operates for both the 'Gain' and 'AcHf' calibration operations. An example using 'KEYBOARD' to calibrate directly against a Standard Cell is shown in the table below.

1.7.2 'KEYBOARD' with Negative Inputs

If the 'KEYBOARD' method is used on DC Voltage calibration with Negative polarity sources, it is important NOT to enter a negative sign with the keyed-in source value. The instrument itself can determine the polarity of the source and update the appropriate calibration memory location.

1.7.3 'KEYBOARD' Calibration Example

The example shown in the table below uses 'KEYBOARD' to calibrate the 1000V AC LF Range Gain at 500V (step 15 of the AC Voltage Calibration table for Option 12).

CALIBRATION EXAMPLE USING 'KEYBOARD'

Step	Calibration Operation	Calibration Source	OMM Setting	'CALIBRATE' Key	DMM Reading After Calibration	Remarks
1	1000V Range Zero	1.00V rms 500Hz	AC,1000	'Zero'	1.00V ±1 digit	
2	Set and Enter Source Value	500.00V rms 500Hz	'KEYBOARD' then 5,0,0,·,0,0	–	0 then +500.00	Lethal voltage present. Increase Calibration Source in 100V steps if possible
3	1000V AC LF Range Gain Calibration	As above	–	'Gain'	500.00V ±1 digit	

1.8 'AUTOCAL' OVER THE BUS

All the calibration procedures covered in this manual can be carried out remotely using Option 50, the IEEE Bus.

Effectively, the five calibration keys are replaced by fiva Bus instructions and these are used instead of the 'CALIBRATE' keys listed in the Calibration tables on previous pages.

An exampla of calibration with the Bus is given in the table below. A completa program listing for the sama calibration operation assuming an HP9825 controller is as follows:—

```
0: dim D$[15]          define 15 character string variable
1: clr 728             send 'device clear' to DVM (interface 7, address 28)
2: wrt 728,"F3R3Q1W1="  program to DC 1V, SRQ Mode 1, Enable Cal.
3: 0→S
4: wrt 728,"G0="       program zero cal. trigger
5: oni 7,"srq"         jump to SRQ service routine on interrupt
6: eir 7,128           enable SRQ interrupts from interface 7
7: if bit ("01XXXXXX",S) check status byte S
   =0;jmp -1           obtained by service routine
8: dsp "Apply 1V &     prompt operator to apply
   CONTINUE"           calibration source on completing zero cal
9: 0→S;stp
10: wrt 728,"G1="      program gain cal. trigger
11: oni 7,"srq"
12: eir 7,128
13: if bit ("01XXXXXX",S)
   =0;jmp -1
14: wrt 728,"T0W0="    program to Internal Trigger, Disable Cal. on completion of gain cal.
15: lcl 728            program DVM to local state
16: stp
17: "srq":rds(728)→S   SRQ service routine to read status byte
18: red 728,D$
19: iret
*7717
```

CALIBRATION EXAMPLE USING THE BUS

Step	Calibration Operation	Calibration Source	DVM Setting	Bus Controller Instruction	DVM Reading After Calibration	Remarks
1	Set DVM to known state	—	In Remote State	'Device Clear'	—	Program DVM to pradetermined state A0C0DXE0F3M0N0 Q0P0Q0R6S0T5
2	Set DVM to DCV, 1V Range, and prepare for calibration	+0.00000V	Calibration key to 'CAL'	'F3R3Q1W1='	—	Program DVM to Function:DC V(F3) Range:1V (R3) SRQ Mode 1 (Q1) Enable Cal. (W1)
3	1V Range Zero	+0.00000V	In Remote State	'G0='	±.00000V	Program 'Zero' cal., SRQ indicatas when calibration operation completed
4	1V Positive Full Range	+1.00000V	In Remota State	'G1='	+1.00000V	Program 'Gain' cal., SRQ indicates when calibration operation completed
5	Set DVM to Internal Trigger, Disable Cal.	—	In Remote State	'T0W0='	—	Program DVM to Internal Trigger (T0), Disable Cal. (W0)
6	—	—	In Local State, Calibration key to 'RUN'	'Local'	—	DVM in normal mode, free-running

SECTION 2

MECHANICAL DESCRIPTION

2.1 GENERAL

The 1061 has been designed to be either rack mounted in a standard 19" rack (3½" (2U) height required) or bench top/portable with integral tilt stand. An exploded view of the instrument is shown in Fig 2.1.

2.2 FRONT PANEL

The front panel incorporates the signal input terminals, range, function, mode, keyboard, compute and power switches and a numeric/legend gas discharge display.

2.3 REAR PANEL

The rear panel incorporates the mains supply, power input socket and fuses, digital and analog output sockets, rear and ratio signal input sockets, rear/front panel signal input selection switch, run/calibrate keyswitch, calibration interval (error) select switch and current option fuse.

2.4 EXTERNAL CONSTRUCTION

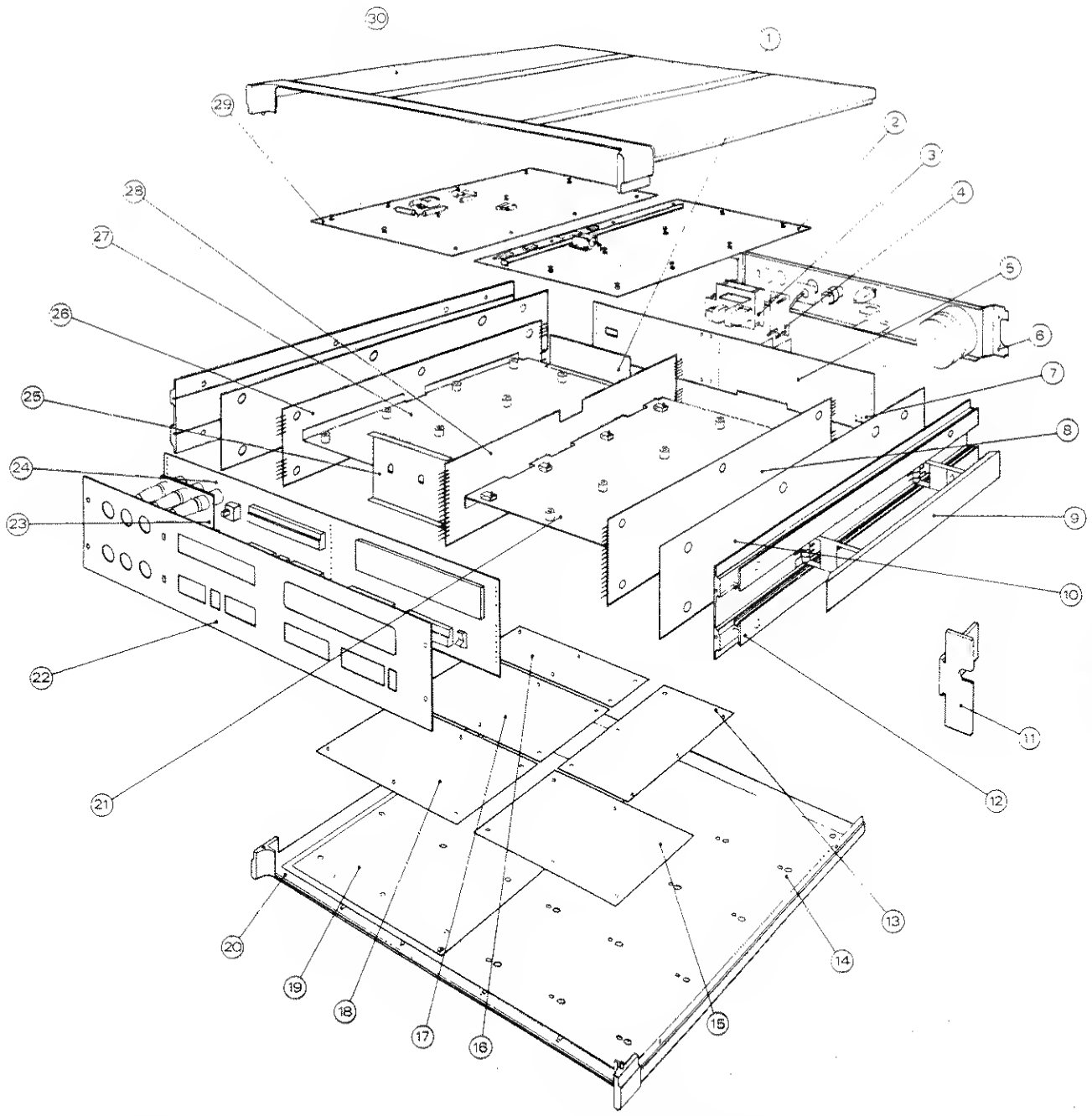
A screen printed key designation overlay adheres to the front panel retaining the polarising filter in front of the display. Both the front and rear panels are held together by two side extrusions running from front to rear. These side extrusions provide both slots for the handles or rack mounting 'ears' and locating points for the structural foam covers. The bottom cover is fitted with the tilt-stand, rubber feet and instruction card. Earth screening of the covers and guarding is provided by aluminium plates, heat-staked to the inside of the covers with electrical connections made by spring contacts.

2.5 INTERNAL CONSTRUCTION

An internal chassis is constructed from five printed circuit boards, held together by connectors at each corner and held rigid by two inner aluminium shields fixed horizontally on the instrument's centre line running from front to rear. Input terminals, switches and display are mounted on the front printed circuit board (pcb) and the power supply on the rear pcb. The two side and centre pcb's are used for interconnections between the main circuit boards.

All the main circuit boards are mounted on the inner shields with hinges and quick release fasteners with flexible connections to allow operation in the 'hinged-up' position. The Analog output circuitry is fixed on to the rear pcb of the chassis and the Ratio/Rear Input circuitry on to the rear panel. The options are mechanically fitted and require no soldering.

The chassis is mounted on to the side extrusions with nylon screws, spacers and an insulation sheet to ensure that the 'electrical spacings' of the BSI, UL and VDE specifications are achieved.



1. REAR GUARD SCREEN
2. DIGITAL ASSEMBLY
3. RATIO/REAR INPUT ASSEMBLY (OPTION)
4. ANALOG OUTPUT ASSEMBLY (OPTION)
5. REAR (POWER SUPPLY) PCB ASSEMBLY
6. REAR PANEL ASSEMBLY
7. POWER SUPPLY VOLTAGE SELECTION LINKS
8. R.H. PCB ASSEMBLY
9. HANDLE ASSEMBLY
10. INSULATION SHEET
11. RACK MOUNTING BRACKET
12. SIDE EXTRUSION
13. DIGITAL INTERFACE ASSEMBLY (OPTION)
14. EARTH SCREEN
15. DISPLAY DRIVER ASSEMBLY
16. CURRENT ASSEMBLY (OPTION) } See Note [1]
17. AC ASSEMBLY (OPTION 10) } See Note [1]
18. OHMS ASSEMBLY (OPTION)
19. OUTER GUARD SCREEN
20. BOTTOM COVER ASSEMBLY
21. R.H. CENTRE GUARD SCREEN
22. FRONT PANEL AND OVERLAY
23. TERMINAL SUPPORT PLATE
24. FRONT PCB ASSEMBLY
25. FRONT GUARD SCREEN
26. L.H. PCB ASSEMBLY
27. L.H. CENTRE GUARD SCREEN
28. CENTRE PCB ASSEMBLY
29. ANALOG ASSEMBLY
30. TOP COVER ASSEMBLY

FIG. 2.1 EXPLODED VIEW OF INSTRUMENT

[1] AC Assembly for 1061A Option 12 is fitted in place of AC Option 10 and Current Option 30 pcb assemblies

SECTION 3

TECHNICAL DESCRIPTION

3.1 INTRDDUCTIDN

The internal circuits of the basic DC only instrument are divided between five printed circuit board assemblies (shown in bold outline in Fig. 3.1).

For the purpose of explanation, each assembly will be described separately and each assembly further sub-divided according to the various functions involved.

3.2 ANALOG ASSEMBLY (Circuit Drawing No. 430328)

The Analog assembly is split into three distinct sections: (i) the Analog Interface, (ii) the DC Isolator and (iii) the Analog to Digital (A - D) Converter.

The Analog Interface receives data from the Digital assembly to control the selection, range scaling and other features of the analog circuitry. Messages between the Analog and Digital assemblies are passed via opto-isolators, electrically isolating one from the other.

The DC Isolator includes the preamplifier, range scaling circuits and bootstrapped supplies. The A - D section converts the scaled input signal to a time period proportional to the signal using a modified triple slope technique.

3.2.1 Analog Interface (430328 sheet 5)

3.2.1.1 Introduction

The Analog Interface provides electrical isolation between the Digital and Analog circuitry. Latched data from the microprocessor is passed through opto-isolators, decoded and latched again on an analog assembly to select function, range, test, average and the D - A converter set up conditions. A line is also provided to instruct the micro-processor which options are present and if the AC assembly is measuring a signal above 5kHz.

3.2.1.2 Power-Dn

At power-on the A - D converter is placed into the RESET condition (See Section 3.2.3.8). The analog circuitry is then interrogated to discern which options (if any) are fitted. Finally the analog circuitry is placed into the DC, 1000V range until a different range or function is selected (See Fig. 3.3).

To determine which options are fitted the Digital assembly sends a series of messages across the isolation barrier, decodes them on the analog side and gates them with lines from the option assemblies to feed a signal back across the isolation barrier to the micro-processor.

Looking at the procedure, in more detail, the Analog Interface Data (ID) lines are all set to a logic '1' except one, which is set to a logic '0', depending on the option being interrogated (See Fig. 3.2). As an example we will check to see if the AC option is fitted. ID1 is set low, the rest of the ID lines set high and the Analog Interface Address lines, IAØ and IA1 set low. The opto-isolators *invert* all signals, thus M17-3 is low and M19 pins 10, 4 and 11 are high. If the AC option is *not* fitted M19-2 is driven low via R55 from M17-3, causing M19-3 to be high, producing a logic '0' (−15 volts) on M18-4. If the AC option *is* fitted a 33kΩ resistor on the AC assembly (R14) overrides R55 and and a high is placed on M19-2. The effect is to produce a

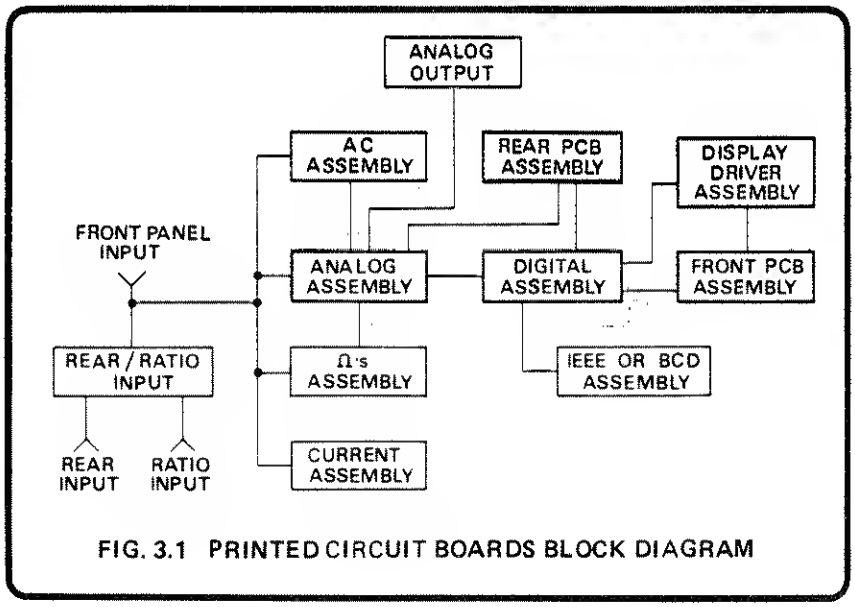


FIG. 3.1 PRINTED CIRCUIT BOARDS BLOCK DIAGRAM

Option checked	ID line low	Pin No. of M19 held low if Option incorporated
AC	ID 1	M19-3
Ω	ID 2	M19-11
I	ID 3	M19-4
RATIO	ID 4	M19-10

Fig. 3.2 POWER-ON OPTIONS FITTED TEST

high on M18-4, turning the opto-isolator M2-B on and thus COND. VAL (M2-B) is high, signalling to the Digital assembly that the AC option is fitted. Similarly, when the Ω, I or RATIO options are interrogated, the appropriate output of M19 is set low if the option is fitted causing the COND. VAL to be set high.

*Note: ID and IA lines
logic '1' ≡ +5 volts logic '0' ≡ 0 volts
AD lines
logic '1' ≡ 0 volts logic '0' ≡ −15 volts

The next step in the power-up sequence as far as the analog circuits are concerned, is to be placed into the DC, 1000V range (See Fig. 3.3 Flowchart). Firstly, all assemblies are deselected by placing logic '1's on all the ID lines, then setting the IAØ and IA1 lines low (see Fig. 3.4), clocking the option selects latches (M20 Analog assembly, M5 AC assembly, M9 Ohms assembly, M1 Ratio assembly from M17-3. Both IA lines then return high.

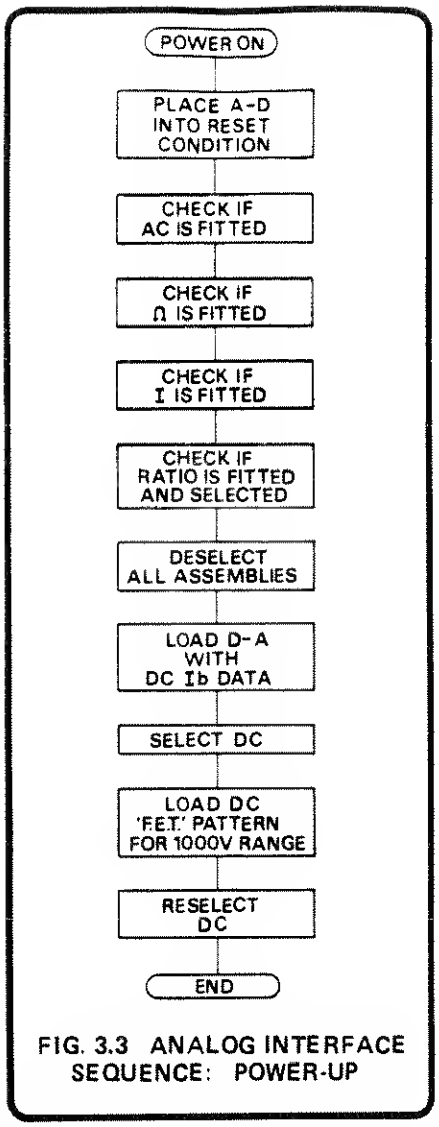


FIG. 3.3 ANALOG INTERFACE SEQUENCE: POWER-UP

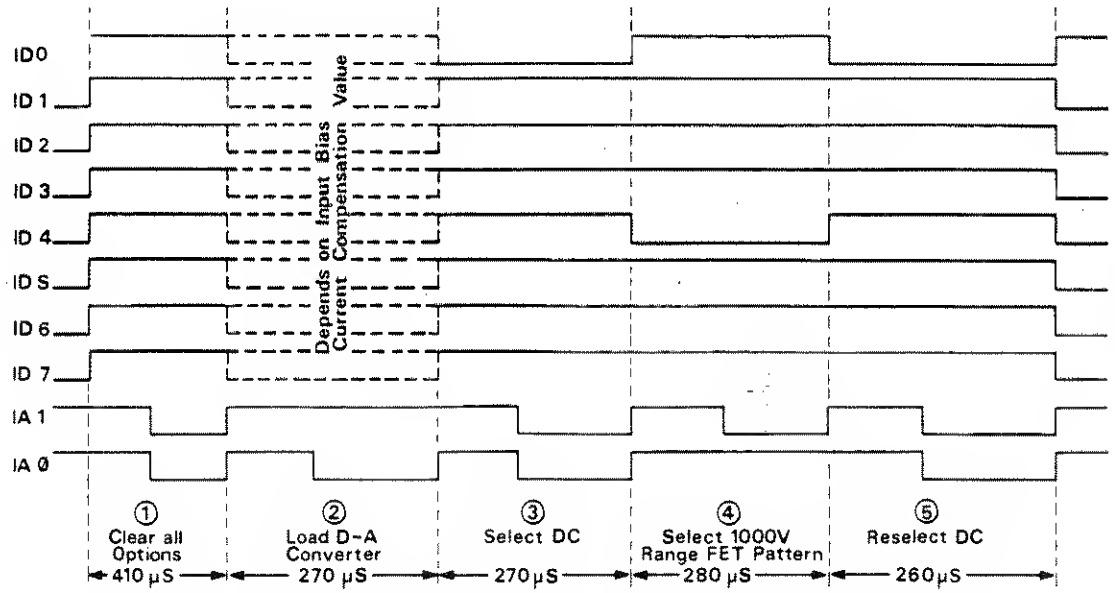


FIG. 3.4 ANALOG INTERFACE DATA LINE TIMING DIAGRAM (POWER-UP)

Secondly, the latches of the D - A converter (M13, M14) are set up with the input bias current (Ib) compensation data. The ID lines are set to the appropriate pattern and the information is clocked on to M13 and M14 by a delayed low to high edge from M17-4, originating from IAØ going low. The delay makes sure that the signal from M17-10 has disabled the "F.E.T." latch M21. Once again, the IAØ line returns to the resting state of logic '1'. Thirdly, the DC analog circuits are enabled by setting all the ID lines high except for ID0, then clocking M20 by a low to high edge from M16-6 caused by both IA lines going low. Once DC has been selected, the F.E.T. pattern latch is enabled from M12-1, and the penultimate step is to load this latch with 1000V range data from the ID lines (ID4 low, the rest high). This is executed by clocking the 'F.E.T.' latch from M17-4 once again, but this time being due to IA1 going low. The final step is to reselect DC as described above.

3.2.1.3 General Interface Update Sequence

Before the start of each reading, the analog interface undergoes a complete update. The series of events is the same as the power-up sequence for selection of function and range, as can be seen by comparing the two flowcharts (Figs. 3.3 and 3.5). When Ohms or Current is selected, the DC Isolator or AC assembly is also used in the measurement procedure as seen in the following table.

Type of Measurement	Circuits Selected	Use of D - A
DC Volts	Analog Assembly	Input Bias Current Compensation
AC Volts	AC Assembly	Frequency Compensation
AC + DC Volts	AC Assembly	Frequency Compensation
Resistance	Ohms Assembly and Analog Assembly	Input Bias Current Compensation
DC Current	Current Assembly and Analog Assembly	Input Bias Current Compensation
AC Current	Current Assembly and AC Assembly	Frequency Compensation
AC + OC Current	Current Assembly and AC Assembly	Frequency Compensation

The update sequence order is (i) Deselect all assemblies, (ii) Load D - A latches, (iii) Select AC assembly or DC Isolator, (iv) Load range pattern into DC or AC range latches, (v) Deselect DC or AC and select either the Ohms or Current assembly, (vi) Load range pattern into Ω's or I range latches, (vii) Reselect circuits selected in (iii) and (iv).

Note: Steps (v) and (vi) are used only when I or Ω is selected.

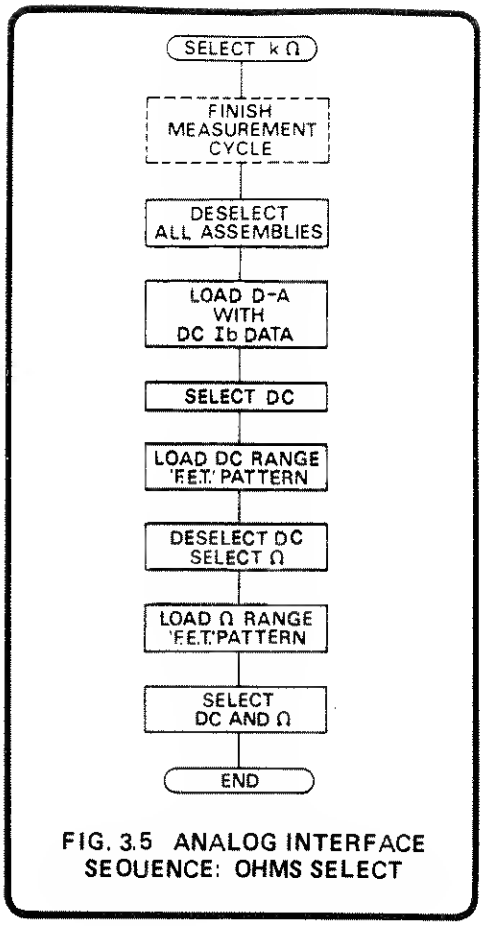


FIG. 3.5 ANALOG INTERFACE SEQUENCE: OHMS SELECT

Flowchart 3.5 gives the above sequence for an ohms update. The general form of the timing diagram for the above sequence is given in Fig. 3.6, the analog 'F.E.T.' patterns for each range of each function being given in Appendix 1.

3.2.1.4 Test

When TEST is selected, a logic '0' is placed on ID7 at stages (iii), (v) and (vii) in Fig. 3.6, i.e. each time a function measurement circuit is selected. Appendix 1 lists the 'F.E.T.' patterns of each assembly for each test measurement cycle.

3.2.2 DC Isolator Section

3.2.2.1 Preamplifier Scaling (430328 sheet 1)

Figure 3.8 shows the essential features of the isolator scaling circuit. For the purpose of explanation the same symbols are used, regardless of whether the switching is accomplished electronically (F.E.T.) or by means of relay contacts. In Fig. 3.8 all switches are shown in the 1V RANGE position.

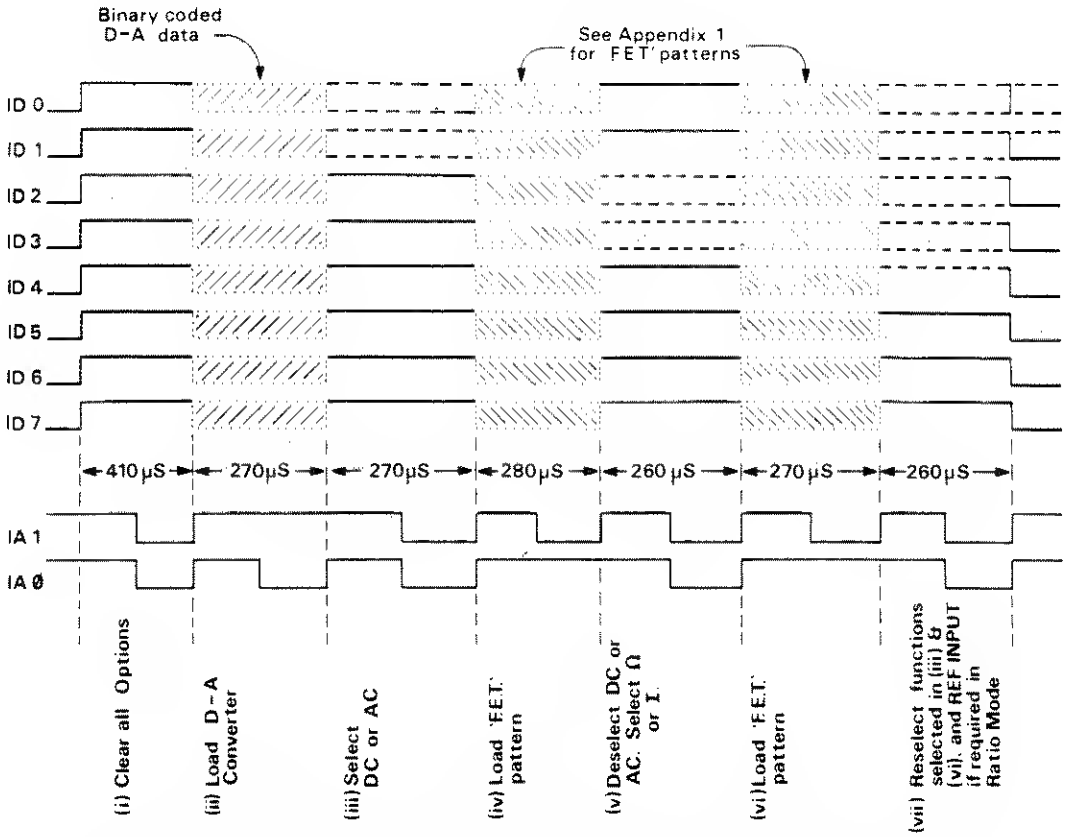


FIG. 3.6 GENERAL FORM OF ANALOG INTERFACE UPDATE TIMING DIAGRAM

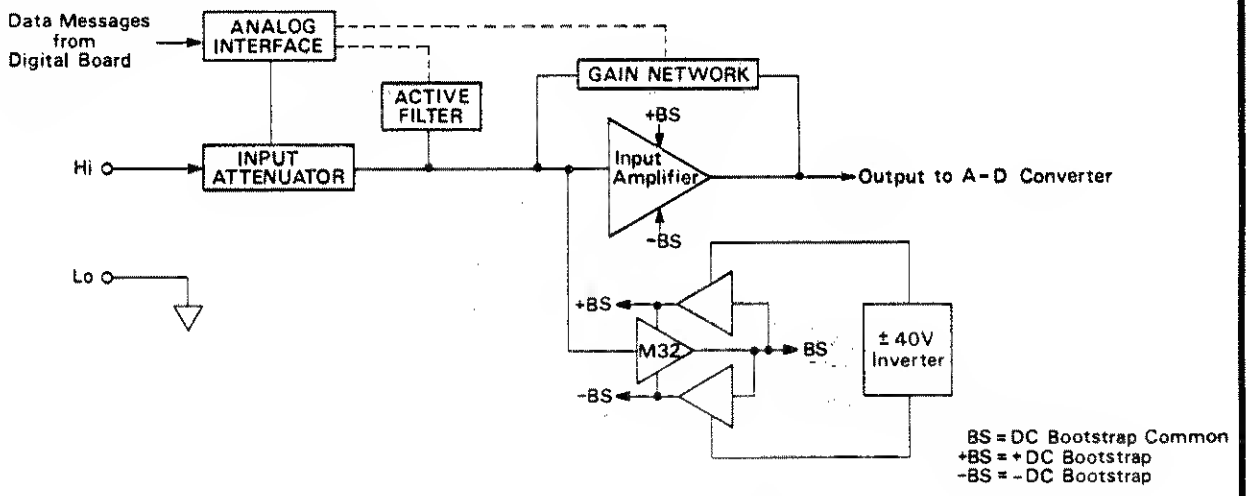


FIG. 3.7 SIMPLIFIED DIAGRAM OF DC ISOLATOR

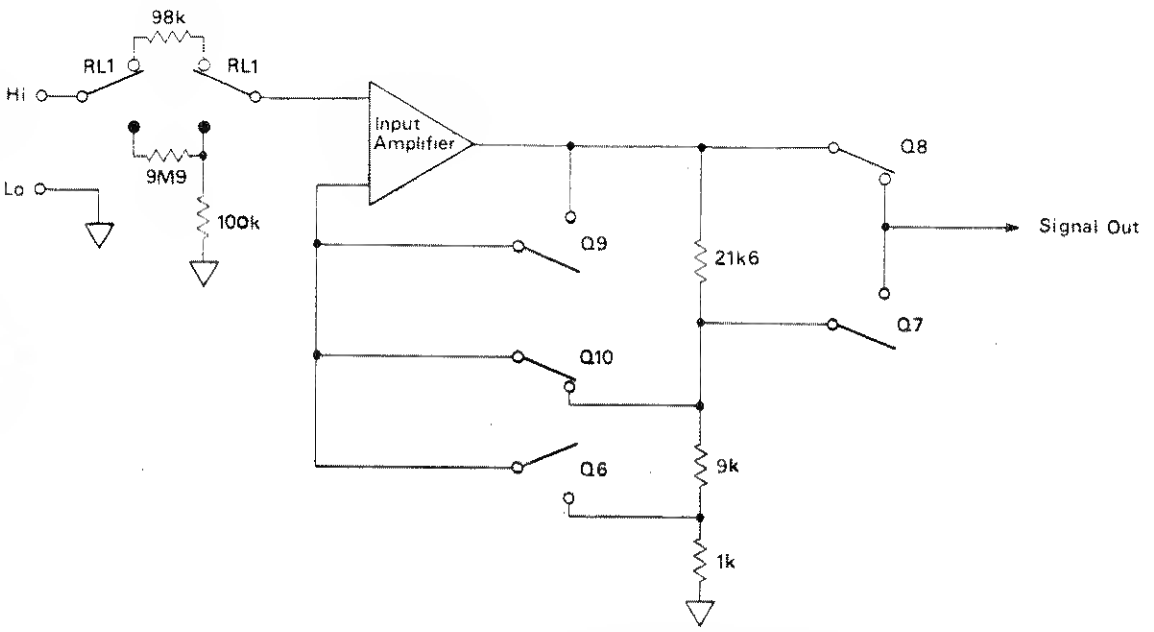


FIG. 3.8 SIMPLIFIED DIAGRAM OF ISOLATOR SWITCHING

The various switching combinations for the different ranges are as follows:—

Range	Gain	Q6	Q7	Q8	Q9	Q10	RL1
100mV	x31.6	ON	OFF	ON	OFF	OFF	ON
1V	x3.16	OFF	OFF	ON	OFF	ON	ON
10V	÷3.16	OFF	ON	OFF	ON	OFF	ON
100V	÷31.6	OFF	OFF	ON	OFF	ON	OFF
1000V	÷316	OFF	ON	OFF	ON	OFF	OFF
$\overline{DC}$		OFF	OFF	OFF	ON	OFF	OFF

The configuration of the circuit for each range is shown in Fig. 3.9.

Reference should be made to circuit diagram number 430328, sheet 1, for the complete circuit. Sheet 2 gives tables of the coding on the input control lines (from the Analog Interface).

When the 100V or 1kV range is selected, a ÷100, 10MΩ input attenuator (R143, R156, R149, R148) is incorporated into the circuit. This is a matched set of resistors for low temperature coefficient. The selection of a lower range energizes relay RL1 (via Q33), causing resistor chain R119-R122 to be in series with the Hi input. Should an overload signal then be applied, the resistor chain limits the current and the power dissipation is such that 1000V can be applied continuously.

The amplifier end of the resistors is clamped by zener diodes D22, D23 and Q18, Q19 to low, thus the amplifier input can never exceed approximately ± 24 volts.

The output from the DC Isolator, test point (TL8) is approximately 3.16 volts ($\approx\sqrt{10}$) for a full range (100,000) input by the following methods (See Fig. 3.9):—

100mV Range Q6 and Q8 are turned on; all other F.E.T.'s are turned off and RL1 energised. Thus the output of the amplifier is connected to its inverting input via R108, R109, R110, R111 and Q6, an attenuator chain of ÷31.6, giving the amplifier an overall gain of X 31.6 Q8 connects the preamplifier directly to the output.

1V Range Q10 and Q8 are turned on, all other F.E.T.'s are turned off and RL1 energised. The output of the amplifier is connected to its inverting input via R108, R109, R110, R111 and Q10, an attenuator chain of ÷3.16, giving the amplifier an overall gain of X 3.16. Q8 connects the preamplifier directly to the output.

10 V Range Q9 and Q7 are turned on; all other F.E.T.'s are turned off end RL1 energised. Q9 causes the emplifier output to be directly connected to its inverting input, giving a gain of unity. The output of the amplifier is attenuated by 3.16 (R114, R115) before being passed to the output via Q7 instead of Q8.

100V and 1000V Ranges These two ranges select the 1V and 10V ranges respectively but a ÷100 attenuator (R149, R156, R143, R148) is inserted between Hi and the preamplifier input when RL1 is de-energised.

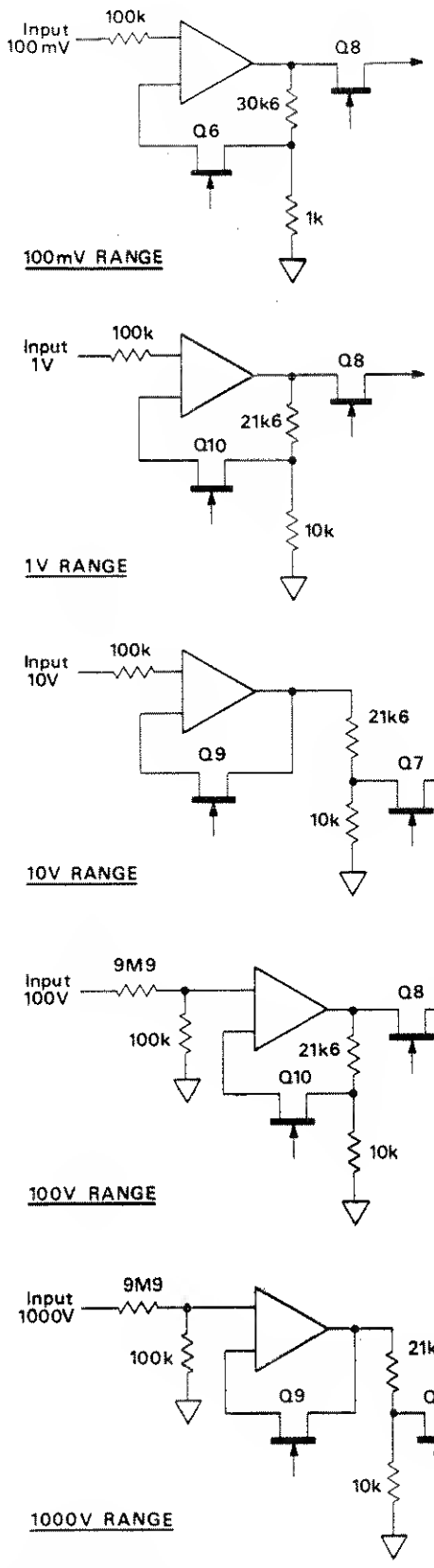


FIG. 3.9 PREAMPLIFIER GAIN CIRCUITS

3.2.2.2 Preamplifier (43032B sheet 1)

The preamplifier is designed to present an input impedance of greater than 10,000MΩ for signals up to ± 20 volts. It is also bootstrapped (tracking of both ground lines and supply voltages with input signal) being essential for correct operation of input bias compensation, temperature compensation and common mode rejection.

Q12 is a well matched monolithic NPN transistor pair exhibiting minimal voltage drift and low noise characteristics, the output being buffered by M31. To compensate for the current gain drift of Q12 (approx. −1%/°C), the change in the base-emitter voltage of one half of Q12 is sensed by M30. The drift compensation is linearised to 1%/°C by thermistor R218. Thus the input bias currant is kept constant with temperature.

3.2.2.3 D.C. Bootstrap (430328 shaet 2)

Bootstrapped supplies are generated which track the input signal directly (BS), track the input signal with a positive offset of +12V(+BS) and track the input signal with a negative offset of −12(−BS).

M32 is the high inpedance buffer which tracks the inverting input of the preamplifier. The offset of M32 is adjusted so that its input is within 100μV of the input of the preamplifier. M32 thus functions as the low impedance rail (BS) following the input signal.

Selection of DC(M20-3) enables the capacitive inverter driven from M33 to provide an unregulated +42V(TL4) and −42V(TL5) supply from the ±15V supply.

The positive bootstrap supply (+BS) is generated as a current source comprising Q26 and the shunt regulator, Q27, referenced to D50. When the output voltage of the regulator is approximately 1.2 volts above D50 cathode, Q27 conducts current into R175. Since the current in R175 is controlled to be constant by Q30, referenced to D50, the current flowing through R174 is reduced. Hence the supply current, "mirrored" in R173, is reduced and the output voltage controlled.

The negative bootstrap supply (−BS) is generated in a similar manner. Thus bootstrapped supplies of approximately ±12 volts are produced, tracking the input signal exactly.

3.2.2.4 Filtering (430328 sheet 1)

Selection of filter causes an active filter to be switched in by relay, RL2, (via Q32). The filter gives an attenuation of −34 dB at 50Hz. The essential components of the filter are shown in Fig. 3.10.

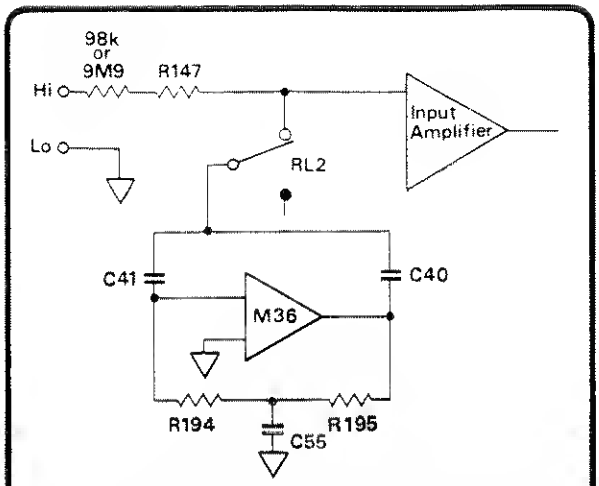


FIG. 3.10 SIMPLIFIED DC ISOLATOR FILTERING CIRCUIT

3.2.2.5 Input Current (Ib) Compensation (430328 sheets 1 and 5)

During the calibration cycle, the microprocessor notes and stores the zero error due to the bias current (measured in a known source resistor). When DC is selected, this information is recalled by the microprocessor, transferred across the isolation barrier and latched into M13 and M14, see Fig. 3.11.

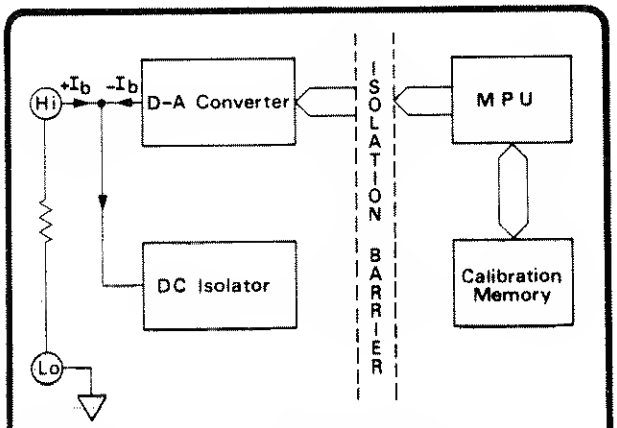


FIG. 3.11 SIMPLIFIED DIAGRAM OF BIAS CURRENT COMPENSATION

The output from the latches is applied to the binary resistor ladder network, AN2, providing a 255 step digital to analog conversion. The analog signal is applied to the inverting input of M3 so that the output drives current, through the diode, to control the current in the corresponding transistor of the opto-isolator, M23. The transistor of the opto-isolator sinks current to the −15V supply until the voltage across R198 is equal to the voltage applied to the inverting input of M3.

The other half of the opto-isolator acts as a current mirror, referenced to the bootstrap (BS) supply. Thus the input current correction is floated on the bootstrap supply, tracking the input signal is divided by R84 to R128 and R129 to null the bias current of the preamplifier.

3.2.2.6 Test (430328 sheets 1 and 5)

During the self-test routine, (actuated from the front panel or remotely programmed) the DC isolator is checked for correct operation. The circuitry is placed into the 0.1V range, as described in 3.2.1.3, except that relay RL1 is not energized, (i.e. the ÷ 100 attenuator is across the input amplifier). Filter is selected and F.E.T. Q5 'closed' via M20-5 causing a small signal to be injected into the feedback path of the input amplifier. Thus a signal of −3.125 volts is output from the DC Isolator (TL8). This signal is then measured and compared with a stored value. If the measured signal is within ±6% of the stored value, the test continues with a 1V range check and a 10V range check.

Range	Output signal from DC Isolator (TP13)
0.1V	− 3.125 volts
1V	− 0.2193 volts
10V	− 0.06932 volts

DC Isolator Output Test Voltages

3.2.3 Analog to Digital Conversion (Analog Section) (430328 sheets 3 and 4)

3.2.3.1 General Principles

Section 1 and Fig. 1.2 of the User's Handbook gives a very basic description of the principles of the integration involved. The technique used in the Autocal Voltmeter is a quadruple slope, the two extra slopes being towards the end of the signal and reference integration periods respectively.

Fig. 3.12 is a simplified diagram showing the essentials of the analog section of the A · D conversion and should be used with timing diagram Fig. 3.13 for full appreciation of the circuit operation.

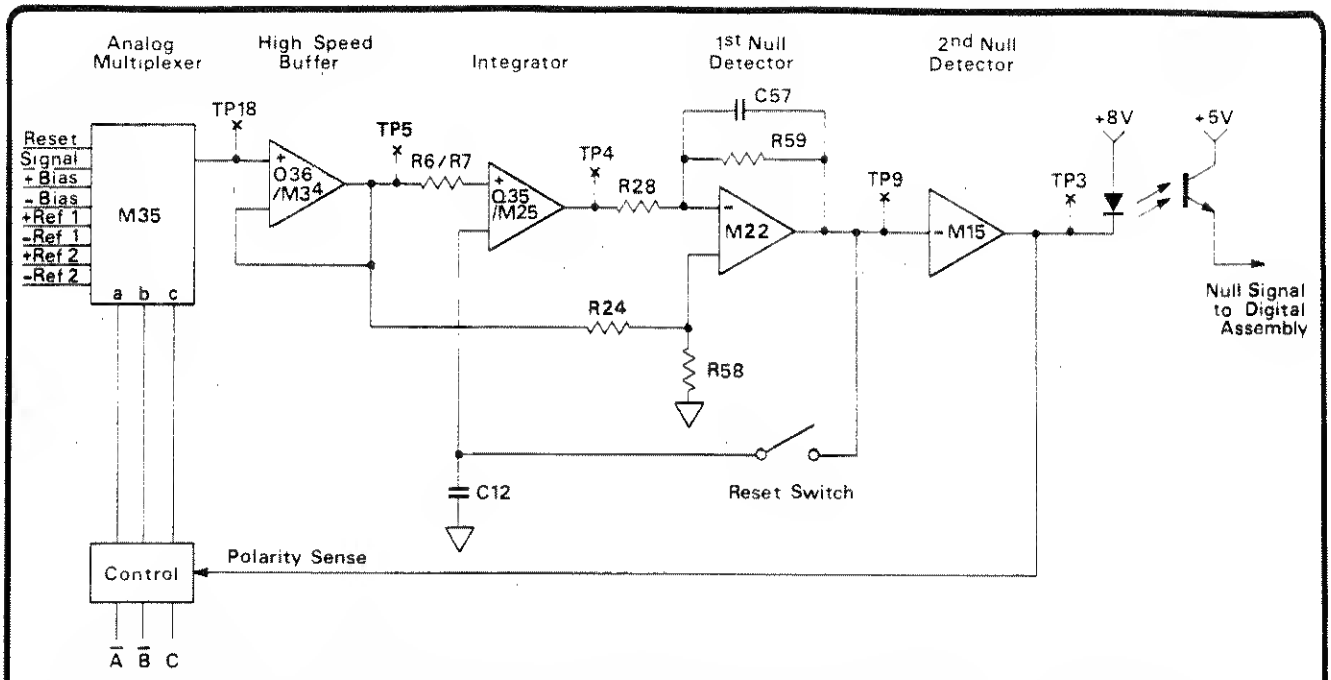


FIG. 3.12 SIMPLIFIED DIAGRAM OF ANALOG SECTION OF A – D CONVERTER

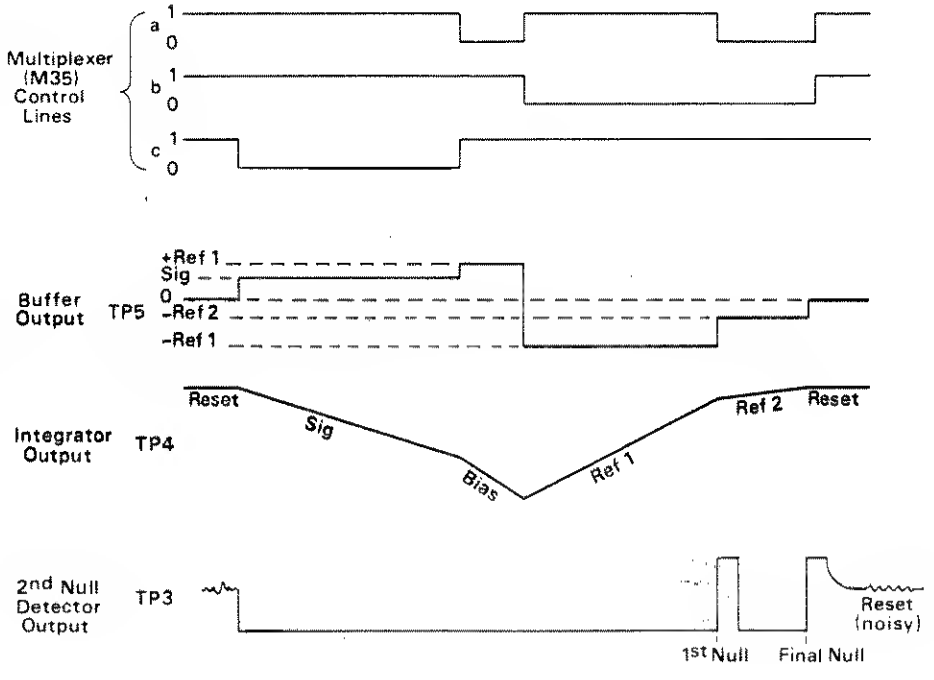


FIG. 3.13 TIMING DIAGRAM FOR ANALOG SECTION OF A – D CONVERTER
(Positive Signal)

3.2.3.2 A - D Input Control

The analog signal from the DC Isolator is applied to the analog multiplexer (M35) and fed to the input of the buffer (Q36/M34). This in turn feeds the signal to the integrator comprising of Q35, M25 and C9.

Control of the multiplexer is derived from the Digital assembly via opto-isolators M4, M5 and M6. These signals control the sequence of events, allowing first the signal, then a bias voltage of the same polarity as the signal, followed by opposite polarity reference and reference ÷16 signals to the buffer and integrator. The multiplexer is then placed in a reset condition ready for the next measurement cycle. Fig. 3.14 gives the multiplexer control line sequence for both positive and negative signals.

STATE	a	b	c	STATE	a	b	c
RESET	1	1	1	RESET	1	1	1
SIG	1	1	0	SIG	1	1	0
+ BIAS	0	1	1	−BIAS	0	1	0
−REF 1	1	0	1	+REF 1	1	0	0
−REF 2	0	0	1	+REF 2	0	0	0
RESET	1	1	1	RESET	1	1	1
	Positive signal				Negative signal		

Logic levels : (0 ≡ −8V, 1 ≡ +8V)

Fig 3.14 MULTIPLEXER CONTROL LINE SIGNALS

3.2.3.3 Reference Voltages and Control Logic Power Supply

REF 1 : The two halves of M39 in conjunction with zener diodes D60 and D59 form the positive and negative reference voltages respectively, D65 and D64 being 'start-up' diodes (see Fig. 3.15). The outputs of M39 (+11 and −11 volts) supply the defined current for the reference zeners via R212 and R38 respectively. R19 and R18 are selected by Datron so that each zener has zero voltage/temperature coefficient.

The resistor chains R42-R43 and R89-R90 are binery weighted values allowing the set up of the exact nominal REF 1 voltages, of ±6.42V, by cutting the appropriate links.

REF 2 : The second reference is 1/16th of REF 1. The positive and negative REF 1 voltages are divided by R71, R68 and R214, R70 respectively.

The power supplies for the logic circuits M35, M29, M27, M28 and opto-isolators M1, M4, M5 and M6 are also derived from M39 via zener diodes D61 and D62, giving supply voltages of ±8 volts.

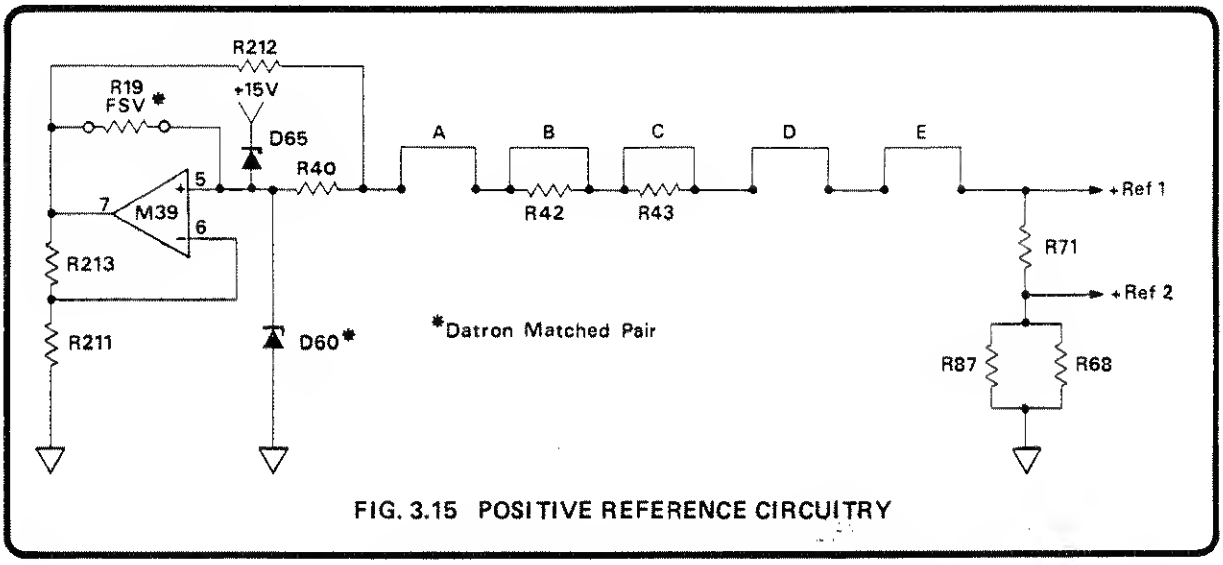


FIG. 3.15 POSITIVE REFERENCE CIRCUITRY

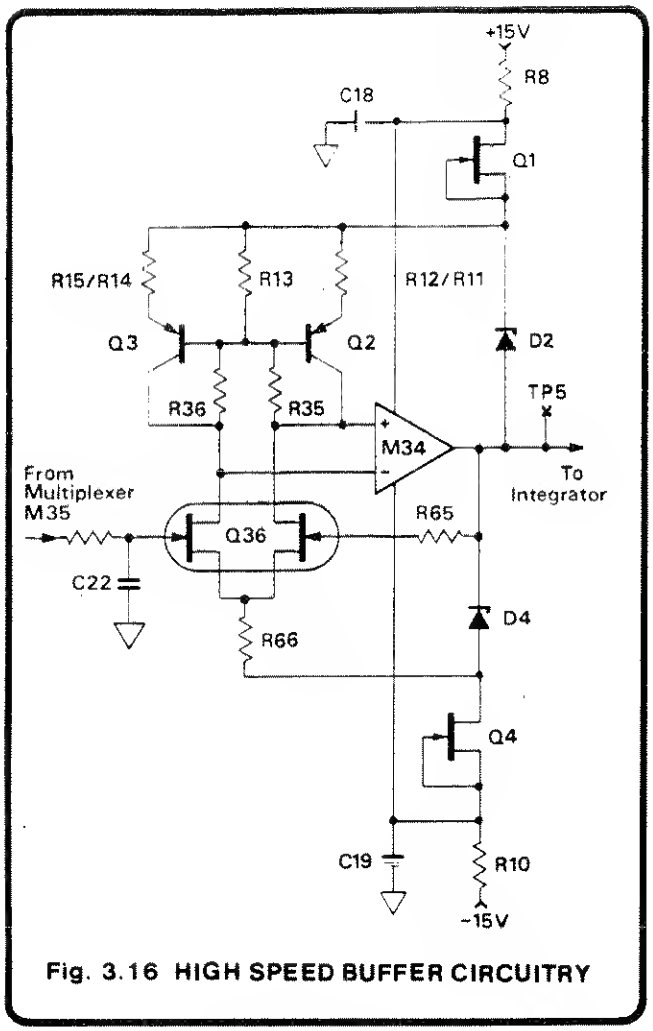


Fig. 3.16 HIGH SPEED BUFFER CIRCUITRY

3.2.3.4 High Speed Buffer

C22 slows the switching edges from the multiplexer M35 so that the buffer cannot slew-limit and thus lose the charge. The signals are fed to Q36, M34 which comprise a high speed buffer with high common mode rejection ratio (See Fig. 3.16). The common mode rejection is dependent on the power supplies of Q36 (from R66 and R11·R15) being bootstrapped to the output of the buffer, via D2 and D4. Thus the difference between input signal and power supply around the input stage is maintained constant whatever the input signal.

3.2.3.5 Integrator

The basic Integrator comprises R6, R7 and C9, with hybrid amplifier Q35 and M25. (See Fig. 3.17). Low-noise FET-pair Q35 also has low gate leakage, which maintains the effectiveness of 'sample-and-hold' components R34 and C12.

An inverted and attenuated version of the integrator output voltage is developed across R5. This is applied via R4 and C10 to compensate for the small amount of dielectric absorption in C9. The value of R5 is factory-selected to equalize readings of the same input, taken at differing read-rates (including 'one-shot' measurements).

C11 and R27 provide shorter term compensation, R23 being set to correct linearity at 10% of full range.

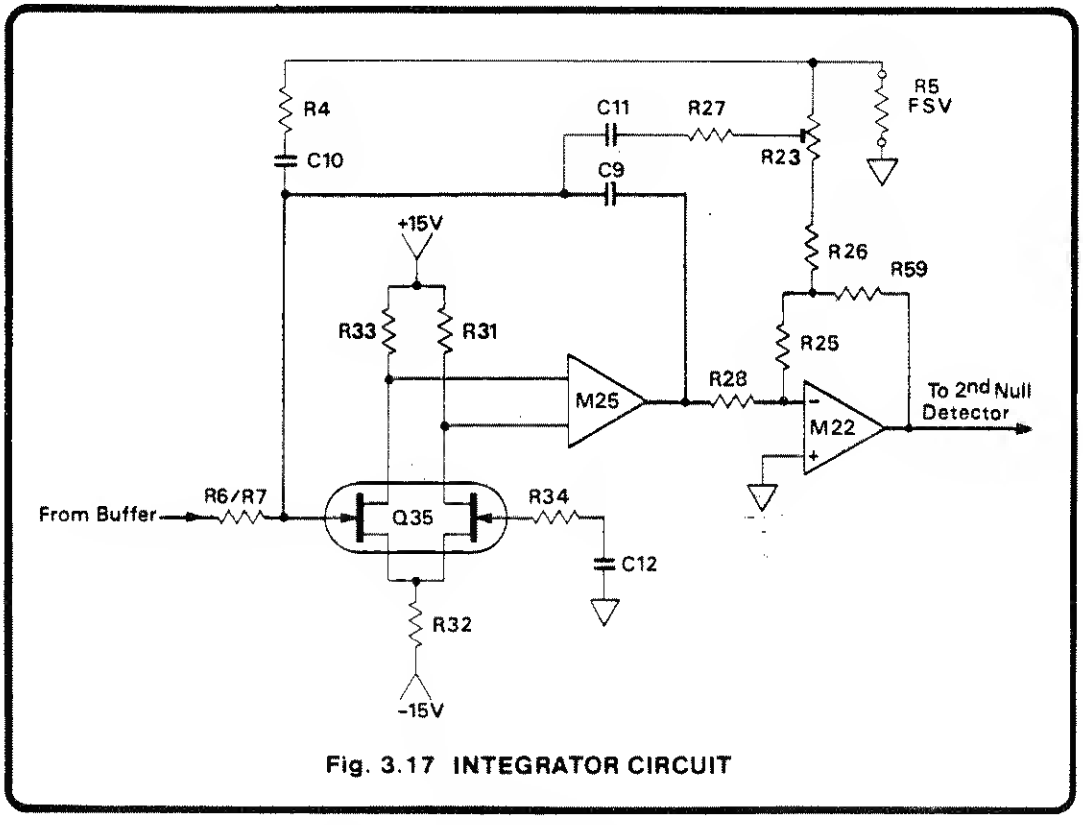


Fig. 3.17 INTEGRATOR CIRCUIT

3.2.3.6 1st Null Detector

The 1st null detector comprises a low noise amplifier, M22, an inverting configuration, where the dc gain is controlled by the ratio of R59 to R28 for small inputs. For larger inputs from the integrator the clamp diodes, D1 and D3, prevent the amplifier from saturating.

During REF 1 the non-inverting input is offset by approximately 10mV to determine the point at which REF 2 is applied (after counting is synchronised). In REF 2 the offset reduces by a factor of 16 giving the null reference point.

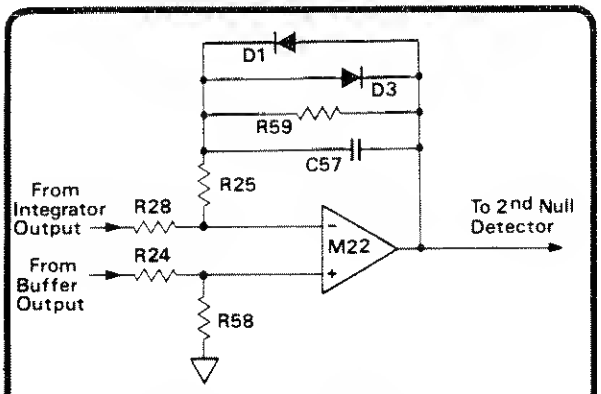


FIG. 3.18 1st NULL DETECTOR CIRCUITRY

3.2.3.7 2nd Null Detector

The signal from the 1st null detector is applied to M15 which boosts the voltage gain. The output provides a logic drive signal via opto-isolator M1, signalling the digital circuitry whenever a null condition changes, Fig. 3.19.

When in an averaging mode (Input Zero or CAL Zero selected; or for 1061A only, with 'Input Filter' and DC, AC Option 12, or Ohms selected) the second null detector is offset a small amount in a cycle of 16 steps (See Fig. 3.20). This offset is produced from the digital to analog converter M28, which is enabled by the level-shifted $\overline{AVE}$ signal from M20-5, and clocked from M6, the C control opto-isolator.

3.2.3.8 Reset Period

At the end of a measurement cycle or in hold, the circuitry is placed into a reset condition. The control lines of the multiplexer M35 allows the 0 volts reference input, at pin 4, to be connected to its output. (See Fig. 3.21). At the same time the reset line (M27-3) is taken high turning on M26. This reset signal, applied to pins 5 and 12 of M26, allows the output of the 1st null detector to be fed back via R60 to a sample and hold capacitor C12 on the integrator.

Thus, with the input to the A - D converter at zero volts, the charge stored on C12 is the sum of all the offsets from the multiplexer, buffer, integrator and 1st null detector, allowing the 1st null detector to indicate the true zero crossing (null) point.

The reset signal applied to M26 pins 6 and 13 merely allows a lower impedance path between the buffer and the integrator to speed up the settling time as C9 is discharged to zero.

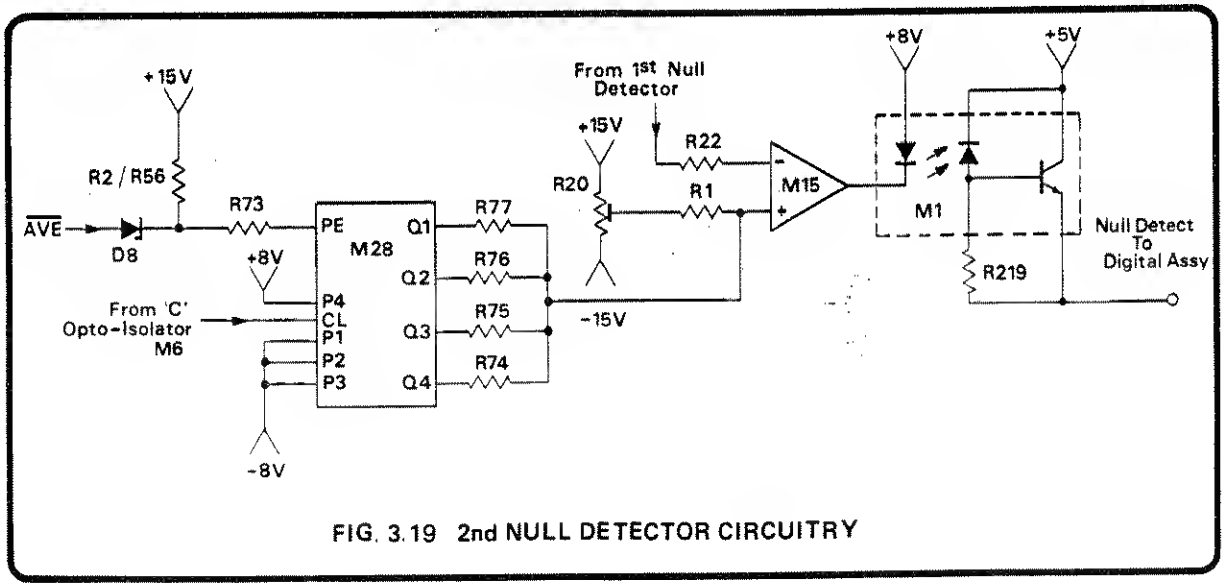


FIG. 3.19 2nd NULL DETECTOR CIRCUITRY

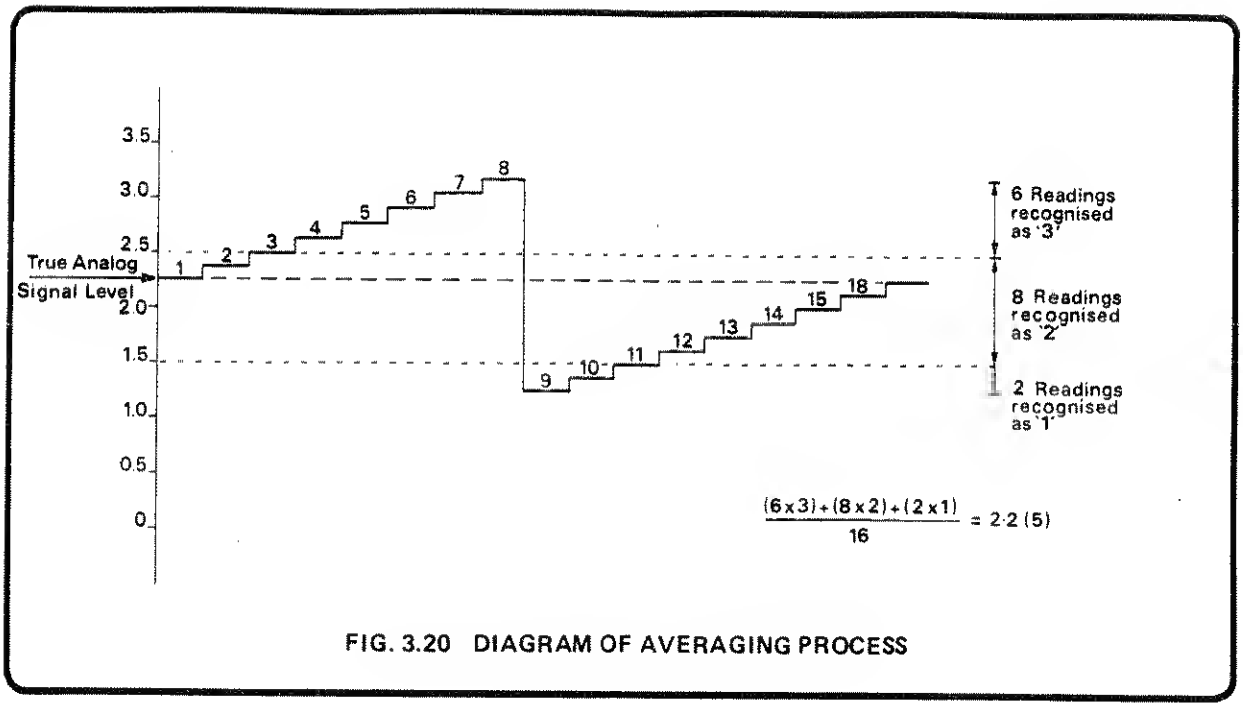


FIG. 3.20 DIAGRAM OF AVERAGING PROCESS

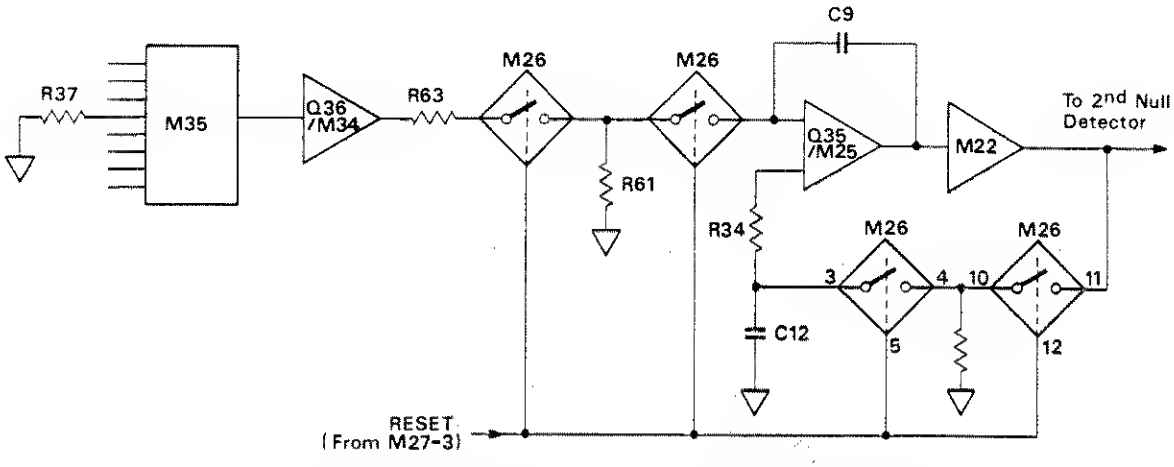


FIG. 3.21 SIMPLIFIED DIAGRAM OF A – D DURING RESET PERIOD

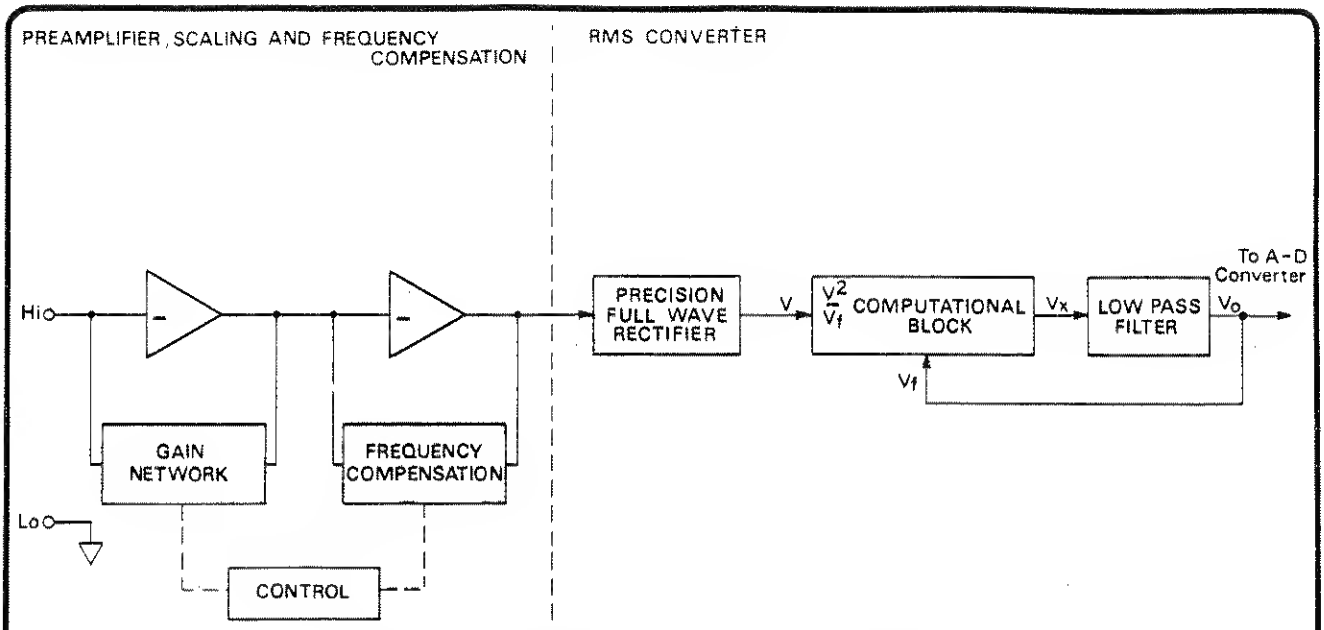


FIG. 3.22 SIMPLIFIED DIAGRAM DF AC CONVERTER

3.3 OPTION 10 AC ASSEMBLY (Circuit Drawing No. 430402)

(For OPTION 12 see page A27)

3.3.1 General Principles

The preamplifier buffers and ranges the signal in order to present 0.9 volts full range to the AC to DC converter section.

Once converted to an equivalent DC signal, it is applied to the analog to digital converter on the main analog assembly.

The conversion technique is electronic true RMS sensing as shown in the simplified block diagram Fig. 3.22. The Datron RMS module can be best considered as a functional block consisting of circuitry which accepts two inputs, V and V_f, computes V^2/V_f and has an output of V_x which is then filtered so that all the AC components are removed. The output of the block is fed back to V_f, thus closing the loop around the whole circuitry.

Mathematically: $\overline{V_x} = V_o$

but $V_x = V^2/V_f$

$\overline{V^2}/V_f = V_o$, but $V_o = V_f$

$\overline{V^2} = V_o{}^2$

i.e. $V_o = \sqrt{\overline{V^2}}$

3.3.2 Preamplifier and Scaling (430402 sheet 1)

Relay RL2 is energised on selection of AC, directly connecting the Hi terminal to the input of the AC assembly. If DC and AC are selected together, the AC assembly becomes DC coupled by energising RL3, causing C57, the AC coupling capacitor, to be by-passed.

The signal is then fed to the switched gain inverting preamplifier whose full range output is 0.9 volts r.m.s. A simplified diagram of this arrangement is shown in Fig. 3.23. The frequency response is held flat, to within ±1%, by controlling the gain defining component time constants, to a similar order of accuracy. Residual errors are removed by the frequency compensation stage. (See section 3.3.4).

The preamplifier has a stable DC path provided by a dual transistor pair Q33 and a fast AC path by dual F.E.T.'s Q32 and Q34. Further gain is provided by the following long-tail pair cascade of Q20, Q21, Q22 and Q23, which is loaded by a current mirror, Q24. Q15 and Q16 with bias components Q17 and Q18 form a conventional class AB output stage. R121 compensates for the bias current of Q33, whileR112 trims the offset voltage to zero.

The unity gain frequency compensation amplifier consists of a stable DC path, provide by M11, and a fast AC path provided by Q25 to Q29. The bootstrap circuit of Q19 presents the varicap diode, D11, with a high impedance, thus ensuring that the varicap is not shunted to ground.

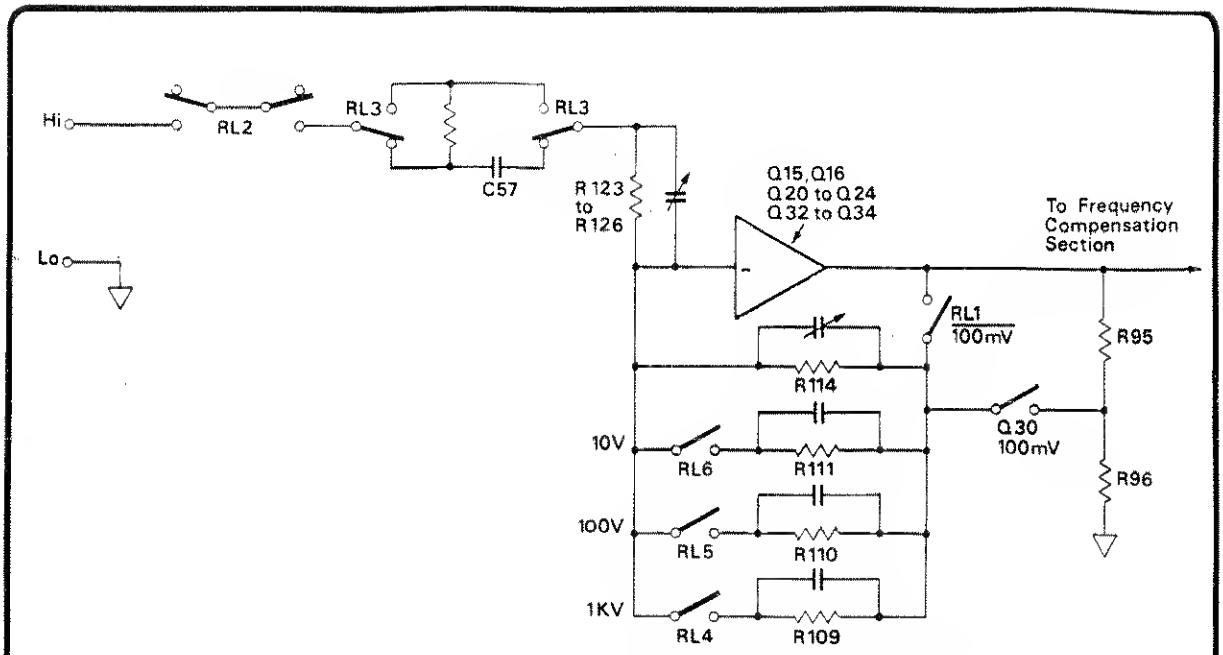


FIG. 3.23 SIMPLIFIEO OIAGRAM OF THE AC PREAMPLIFIER SCALING

3.3.3 RMS Converter (430402 sheet 2)

The RMS converter takes the scaled AC signal from the preamplifier and converts it to an equivalent DC signal suitable for Analog-to-Digital conversion. The conversion technique is electronic true RMS sensing as shown in the simplified block diagram Fig. 3.25.

M8 and M9 form a summing type, full wave rectifier. The output of M8, a precision half-wave rectifier inverter, is summed with the non-inverted signal with a weighting of 2 : 1 at the input of M9. This forces a full-wave rectified current to flow in RMS module M6. Potentiometer R50 balances the rectifier to provide the same output for non-inverted or inverted asymmetric waveforms.

The output current from the RMS module passes into filter-buffer M1 and is converted to a nominal 5 volts for a full range signal. Q1 and Q2 switch in additional capacitors when FILTER is selected, to operate down to 45Hz. M2 is a voltage to current converter providing a feedback current to the RMS module proportional to the output voltage. R90 is the zero adjustment for the half wave rectifier M8 and R35 is the high crest factor gain adjustment. R75 is adjusted for optimum linearity.

The output of M1 (TP2) is fed to a resistor chain R1 - R7, to provide an output of 3.14 volts by the selection of resistors R2 - R5. O3 is turned on when AC is selected and switches the output of the AC converter into the Analog-to-Digital Converter (Drawing No. 430328 sheets 3 and 4).

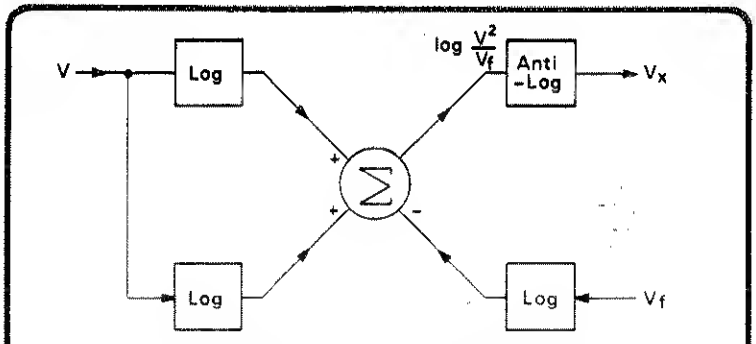


FIG. 3.25 BLOCK OIAGRAM OF RMS CONVERSION TECHNIOUE

3.3.4 High Frequency Compensation

During the calibration cycle, the microprocessor notes and stores the high frequency (HF) error of each range. When AC volts is selected the compensation information for a particular range is recalled by the microprocessor, transferred across the isolation barrier and latched on to M13, M14 (Drawing No. 430328 sheet 5), see Fig. 3.26. As in the case of the Input Current Compensation (section 3.2.2.5), the output from the latches is applied to a digital-to-analog converter, AN2. The voltage produced is fed to the AC converter via connector J1 pin 11 and applied to varicap D11. The varicap is thus adjusted to give the amplifier chain a flat frequency response.

The calibration is carried out at one H.F. frequency but since it flattens the AC amplifier response, the correction is valid for all specified frequencies. It should be noted that the calibration routine is iterative since the varicap is non-linear.

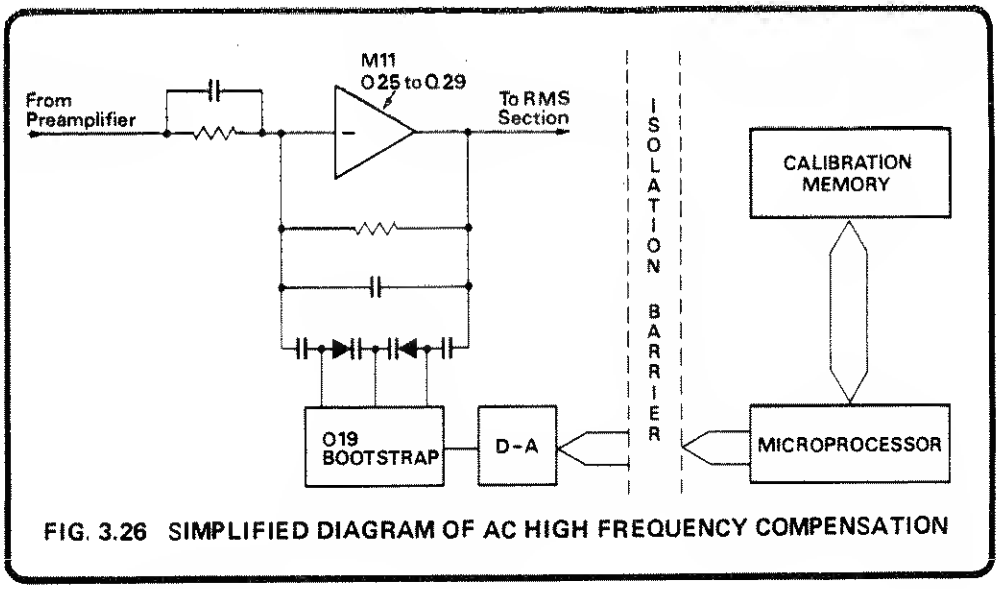


FIG. 3.26 SIMPLIFIED DIAGRAM OF AC HIGH FREQUENCY COMPENSATION

3.3.5 Frequency Detection (430402 sheet 2)

The signal frequency is monitored by M10 which is set so that a signal frequency greater than 5kHz causes a logic '1', (0 volts) on M10 - 4. This signal indicates to the Digital Board via M18, M2 (Drawing No. 430328 sheet 5) which one of the two sets of specifications should be used for calculating the measurement uncertainty when the Spec key is depressed.

3.3.6 Test

During the self-test routine (actuated from the front panel or remotely programmed) the AC assembly is checked for correct operation. The circuitry is placed into the .1V range as described in Section 3.2.1.3. Filter is selected and F.E.T. Q31 is 'closed' from M5 - 13 causing a signal of 0.08 volts DC to be injected into the preamplifier. Thus a signal of approximately 3.14 volts is output from the RMS section and applied to the A - D converter situated on the Analog assembly. This signal is then measured and compared with a stored value. If the measured signal is within ±8% of the stored value, the test continues with a 1V range check.

Range	Output from RMS section
.1	+3.14 volts
1	+0.314 volts

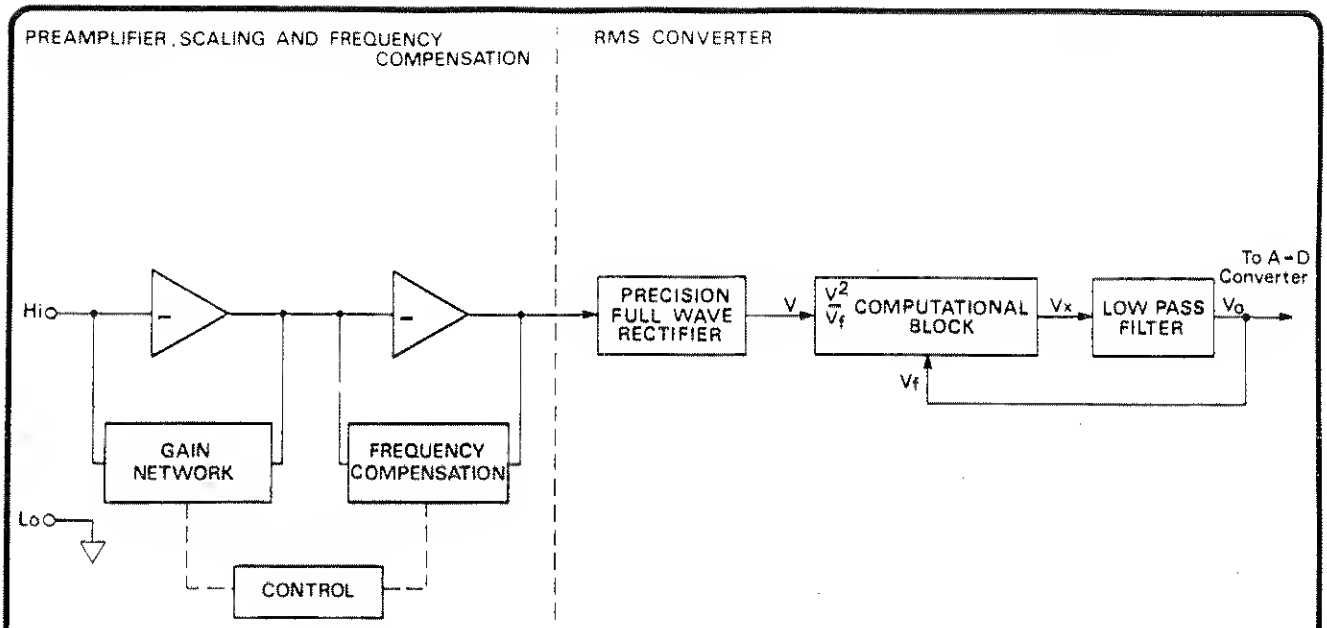


FIG. A3.22 SIMPLIFIED DIAGRAM OF AC CONVERTER

A3.3 OPTION 12 AC ASSEMBLY (Circuit Drawing No. 430552)

(For OPTION 10 see page 27)

A3.3.1 General Principles

The preamplifier buffers and ranges the signal in order to present 0.9 volts full range to the AC to DC converter section.

Once converted to an equivalent DC signal, it is applied to the analog to digital converter on the main analog assembly.

The conversion technique is electronic true RMS sensing as shown in the simplified block diagram Fig. A3.22. The Datron RMS module can be best considered as functional block consisting of circuitry which accepts two inputs, V and V_f, computes V^2/V_f and has an output of V_x which is then filtered so that all the AC components are removed. The output of the block is fed back to V_f, thus closing the loop around the whole circuitry.

Mathematically: $\overline{V_x} = V_o$

but $V_x = V^2/V_f$

$\overline{V^2}/V_f = V_o$, but $V_o = V_f$

$\overline{V^2} = V_o^2$

i.e. $\underline{V_o = \sqrt{\overline{V^2}}}$

A3.3.2 Preamplifier and Scaling (430552 sheets 1 & 2)

When the AC option is selected, the AC preamplifier is connected in parallel with the 1000 Volt range of the DC isolator. The resultant impedance presented at the input terminals is a resistance of 1MΩ, shunted by 150pF.

Relay **RL2** is energized on selection of AC, directly connecting the Hi terminal to the input of the AC assembly. If DC and AC are selected together, the AC assembly becomes DC coupled by energizing **RL3**, causing C77, the AC coupling capacitor, to be by-passed.

The signal is then fed to the switched gain inverting preamplifier whose full range output is 0.9 volts r.m.s. A simplified diagram of this arrangement is shown in Fig. A3.23. The frequency response is held flat, to within ±1%, by controlling the gain defining component time constants, to a similar order of accuracy. Residual errors are removed by the frequency compensation stage. (See section 3.3.4).

The main amplifier M22 responds to signals from DC to above 1MHz. Its input buffer Q36 reduces bias current errors. A chopper-stabilized amplifier M21 nulls the offset of Q36. Filter components R123 and C90 eliminate the effects of current 'kickback' from M21 to the main signal path. M22 output (Test link TLK) is fed directly to the unity gain frequency compensation stage.

C88 and C89 decouple R160 and R162 except on the 100mV range, when Q33 and Q34 are switched off to provide greater open loop gain. To ensure stability at the higher feedback levels required for the 10V, 100V, and 1000V ranges; C73 is switched in by Q32 to decouple M22 non-inverting input, further reducing the open loop gain.

The unity gain frequency-compensation amplifier includes a stable DC path M20, and a fast AC path Q28 and Q29. The capacitance of varicap diode D14 is determined by the bias voltage at J1-11. The bootstrap circuit of Q17/Q21 ensures that both halves of the varicap are subjected to the same AC signal, removing the non-linearity of the voltage-capacitance characteristic.

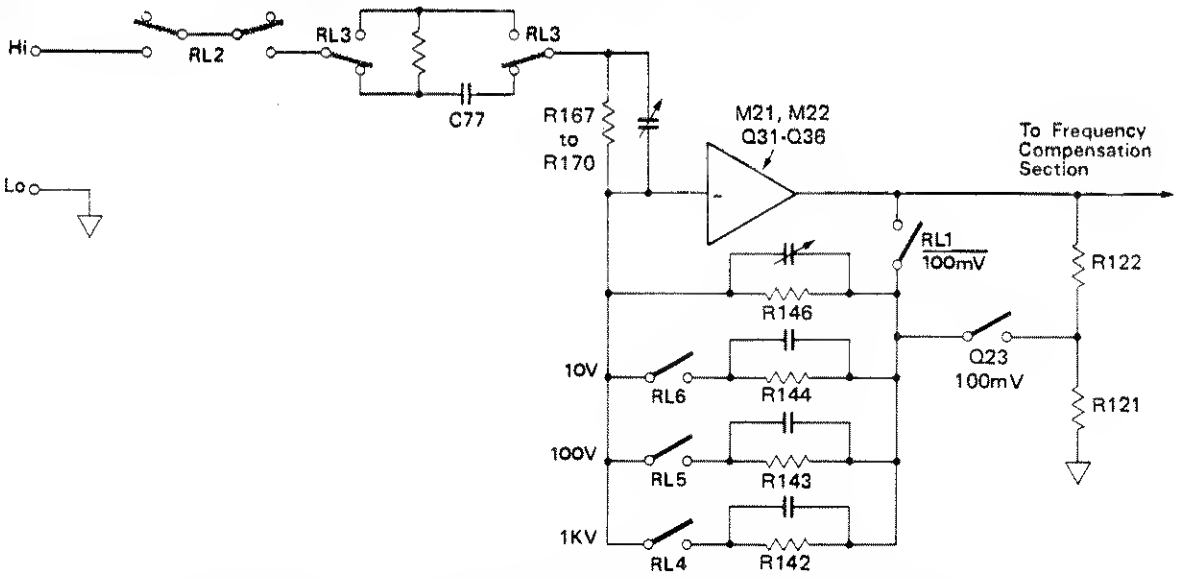


Fig. A3.23 SIMPLIFIED DIAGRAM OF THE AC PREAMPLIFIER SCALING

A3.3.3 RMS Converter (430552 Sheets 2 & 3)

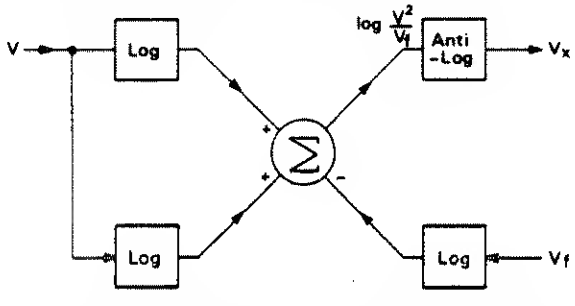


Fig. A3.25 BLOCK DIAGRAM OF RMS CDNVERSION TECHNIOUE

The RMS converter takes the scaled AC signal and converts it to an equivalent DC signal suitable for Analog-to-Digital conversion. The technique used is Electronic True RMS Sensing as shown in the simplified block diagram Fig. A3.25.

M13 and M14 form a summing full-wave rectifier. The output of precision half-wave rectifier M13 is summed with the non-inverted signal at the input of M14, with a weighting of 2:1. This forces an accurately rectified full-wave current to flow in RMS module M11. Potentiometer R62 adjusts the rectifier symmetry to provide the same output for signals of either polarity.

The output current from the RMS module drives the low pass current-to-voltage converter M10/M13, which generates a nominal 0.5 Volts for a full range signal. (Note that M10, M9 and M4 ara chopper-stabilized amplifiers to handle the low signal voltages).

M16 is the active element of a switched 3-pole Bessel filter. M15 and M17 switch the time constants, extending the overall low-frequency response down to 10Hz (See Fig. A3.24), when 'Filter' is selected.

The high impedance output from the 3-pole filter is buffered by M9/M2, and the other half of M2 provides a bootstrap for M9 input. D26 and D16 prevent the voltage on TL A from exceeding the +5V power rail, providing overload protection.

The buffer output voltage (3.12V full range) is developed across R52-R56 and R70, referred to Output Common at M4 input. Log-feedback stage M4/M3 closes the 'Square-Root' loop, providing feedback current for the RMS computation in M11.

When the AC, or DC-coupled AC option is selected, Q3 connects the buffer output to the Analog-to-Digital converter. Test links TLC, D, E and F are selectively removed at manufacture to set the correct output level.

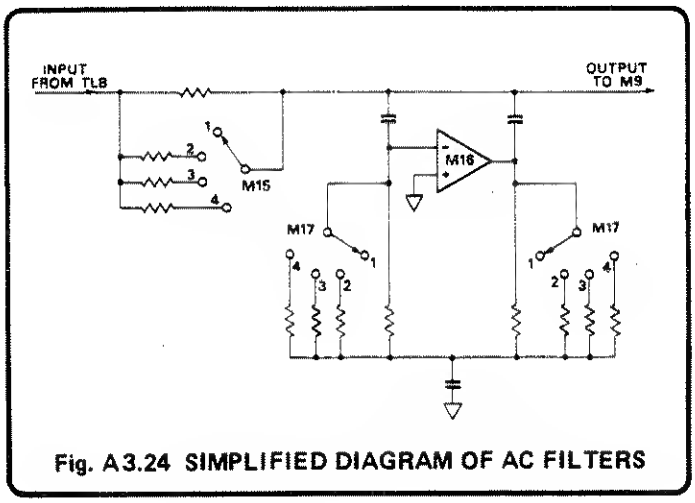


Fig. A3.24 SIMPLIFIED DIAGRAM OF AC FILTERS

A3.3.4 High Frequency Compensation

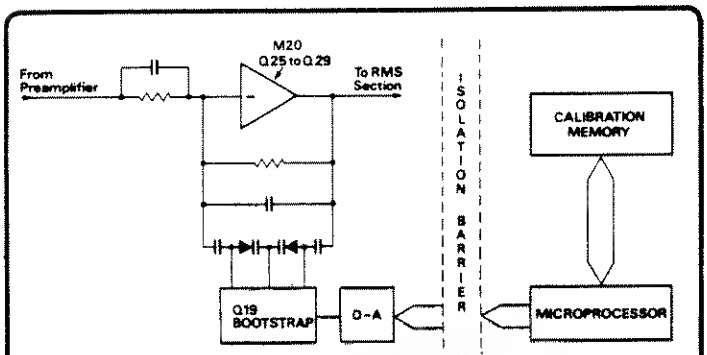


Fig. A3.26 SIMPLIFIED DIAGRAM OF AC HIGH FREQUENCY COMPENSATION

During the calibration cycle, the microprocessor notes and stores the high frequency (HF) error of each range. When AC volts is selected the compensation information for a particular range is recalled by the microprocessor, transferred across the isolation barrier and latched on to M13, M14 (Drawing No. 430328 sheet 5), see Fig. 3.26.

The output from the latches is applied to a digital-to-analog converter, AN2. The voltage produced is fed to the AC converter via connector J1 pin 11 and applied to varicap D14. The varicap is thus adjusted to give the amplifier chain a flat frequency response.

The calibration is carried out at one H.F. frequency but since it flattens the AC amplifier response, the correction is valid for all specified frequencies. It should be noted that the calibration routine is iterative since the varicap is non-linear.

A3.3.5 Frequency Detection (430552 sheet 2)

The signal frequency is monitored by M10 which is set so that a signal frequency greater than 2kHz causes a logic '1', (0 volts) on M19-4. This signal indicates to the Digital Board via M18, M2 (Drawing No. 430328 sheet 5) which one of the two sets of specifications should be used for calculating the measurement uncertainty when the Spec key is depressed.

A3.3.6 Test

During the self-test routine (actuated from the front panel or remotely programmed) the AC assembly is checked for correct operation. The circuitry is placed into the .1V range as described in Section 3.2.1.3. F.E.T. Q31 is 'closed' from M7-13 causing a signal of 0.08 volts DC to be injected into the preamplifier. Thus a signal of approximately 3.14 volts is output from the RMS section and applied to the A - D converter situated on the Analog assembly. This signal is then measured and compared with a stored value. If the measured signal is within ±6% of the stored value, the test continues with a 1V range check.

Range	Output from RMS section
.1	+3.14 volts
1	+0.314 volts

3.4 OHMS ASSEMBLY (Circuit Drawing No. 430331)

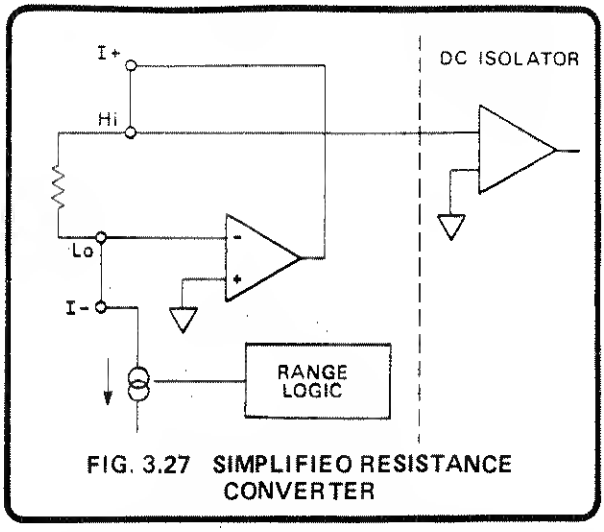


FIG. 3.27 SIMPLIFIED RESISTANCE CONVERTER

The instrument functions by measuring the voltage across an unknown resistance with a known constant current flowing in it. The converter can be split into two parts: a low drift voltage follower and a constant current source covering 6 decades from 100nA to 10mA (see Fig. 3.27).

It should be noted that when the Ohms assembly is fitted the DC Isolator Lo is no longer directly connnected to the front/rear panel Lo terminal, but goes via RL1 on the Ohms assembly (connector link removed on side panel). Lo becomes an active terminal in resistance measurements.

3.4.1 Low Orift Voltage Follower

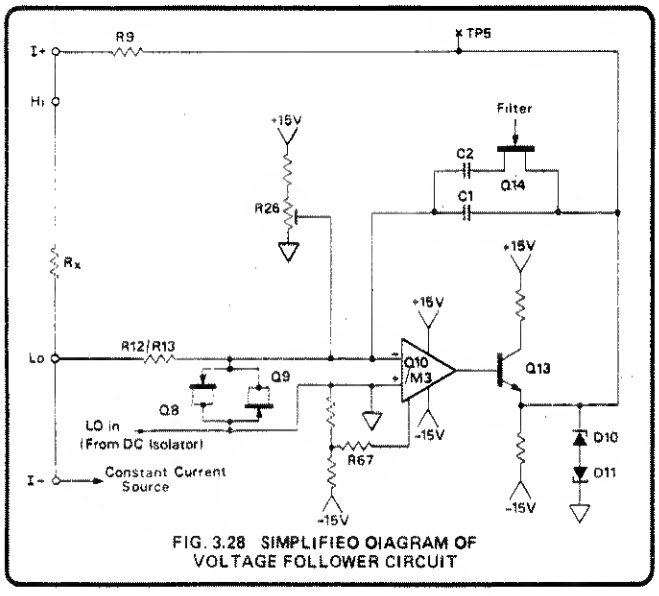


FIG. 3.28 SIMPLIFIED DIAGRAM OF VOLTAGE FOLLOWER CIRCUIT

When OHMS is selected, the front panel Lo terminal is connected to the –ve input of amplifier Q10/M3, the +ve input being referred to DC isolator Lo (this remains reference common). Q10/M3 together with output follower Q13, will thus apply a voltage at the I+ terminal via RL1 such that the voltage at front panel Lo is at reference common plus any offset due to Q10/M3. This voltage offset drift is kept small for changes of temperature by compensating the input bias current of Q10 with the current in R67, which changes with temperature due to the voltage drift at Q10 emitters. Q10 input bias current is initially nulled by R26.

Thus if we consider 2-wire measurement, I+ is linked to Hi, I– is linked to Lo and the unknown resistance linked between Hi and Lo, with a constant current flowing from I+/Hi, through the unknown resistance (R_x) to Lo/I–. The Lo terminal is maintained at 0V. Therefore the Hi terminal (DC Isolator Input) is at $I_{constant} \times R_x$ volts above Lo. As long as the error is small referred to reference 0, the DVM will read the correct resistance.

Input protection is provided as follows:–

Voltage/Current applied to input terminals:

I+	R9, D10, D11
I–	R2, D1, D2, Q25, R23
Lo	R12, R13, Q8, Q9

Open circuit voltage limit protection:

I+	R15, R16, Q6, Q7
I–	R6, D7, D8, Q2, Q22

3.4.2 Constant Current Source

Seven decades of ohms ranges are provided by 6 ranges of current and 2 ranges of DC Isolator voltage gain (100mV range for 10Ω, 1V range otherwise). See Fig. 3.29.

When kΩ's is selected, Q17 (sheet 2) is turned on enabling astable M6 to produce a 200Hz signal to switch M5. Thus when gates B and C of M5 are open, C9 is charged up from the negative reference (originating from the analog section of the A - D converter). These gates then close and A and D open, sharing the charge with C8, the voltage across C8 equals the reference voltage (sheet 1).

Range	Current	F.E.T.'s/Switches turned on	
		Current Selector	Leakage path
10Ω	10mA	Q11, M2(A)	
100Ω	10mA	Q11, M2(A)	
1kΩ	1mA	M1(A)	
10kΩ	100μA	M1(B)	
100kΩ	10μA	Q4	M2(B)
1MΩ	1μA	Q1, M1(D)	Q3, M2(C)
10MΩ	100nA	Q1, M1(C)	Q3, M2(C)

FIG. 3.29 OHMS CURRENT RANGE SWITCHING

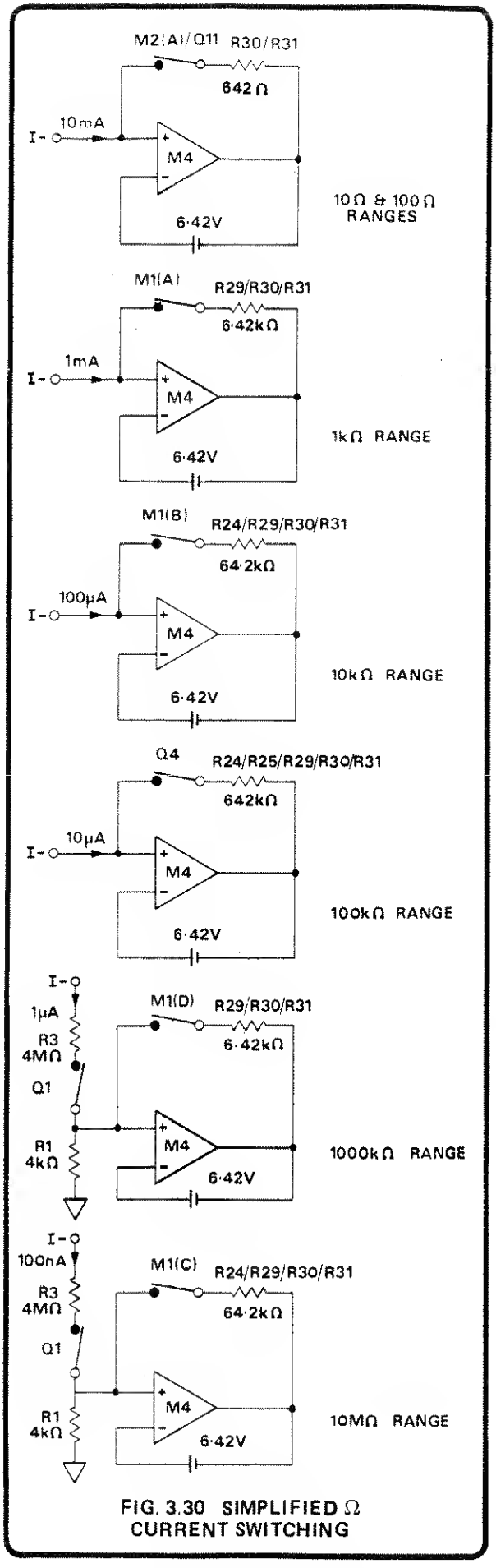


FIG. 3.30 SIMPLIFIED Ω CURRENT SWITCHING

The voltage developed across C8 causes M4 to sink current through resistor chain R24, R25, R29, R30, R31 until the voltage developed across the chain balances that across C8. Thus the current required for a particular range is selected by the value of the resistor chain switched byM1, M2 and Q4. Simplified diagram Fig. 3.30 shows the resistor chain and switching for each range. On the high resistance ranges leakage paths are provided by Q3, M2(B) and M2(C).

To produce good common mode rejection, M4 supplies are bootstrapped, the supply span being defined by a 12 volt zener, D17. The filtered bootstrap supplies (+ΩBS and −ΩBS) power the astable (M6) and bilateral switch.

The use of ohms guard permits in-circuit measurement of resistors, provided shunt paths are greater than 250Ω and a suitable tapping point is available. Consider Fig. 3.31. Guard is reference 0, Lo is actively maintained within microvolts of reference 0 (as previously explained). Thus there is no voltage across Rz and consequently no current in Rz. Voltage follower Q10/M3 will simply pass more current into Ry from the I+ terminal until the selected current for the particular range flows through Rx.

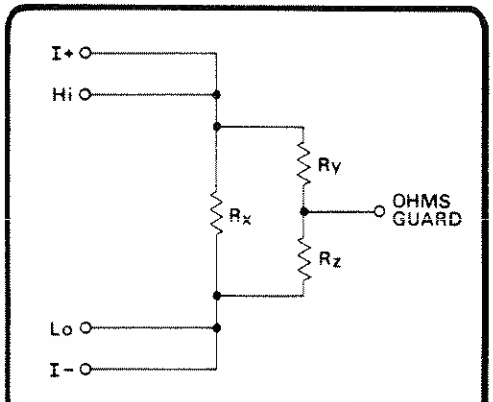


FIG. 3.31 USE OF OHMS GUARD

3.4.3 Test

During the self-test routine (actuated from the front panel or remotely programmed), the Ohms Converter is checked for correct operation. The circuitry is placed into the 10kΩ range as described in Section 3.2.1.3. Filter is selected and F.E.T. Q5 'closed' from M9-1 causing RB (9.76kΩ) to be placed between I+ and I−. Thus with I+ and Hi, I− and Lo connected (2-wire if front panel input selected), the DC Isolator (which is also in the TEST mode) measures the voltage developed across the resistor (approx 1 volt). The resulting voltage output from the DC Isolator is applied to the A-D converter, measured and compared to the stored value. If the measured signal is within ± 6% of the stored value, the test is complete.

3.5 CURRENT ASSEMBLY (Drawing No. 430304)

The Current assembly contains a set of selectable precision current shunts, the voltage developed across the shunt(s) being sampled by the DC or AC voltage measurement circuits.

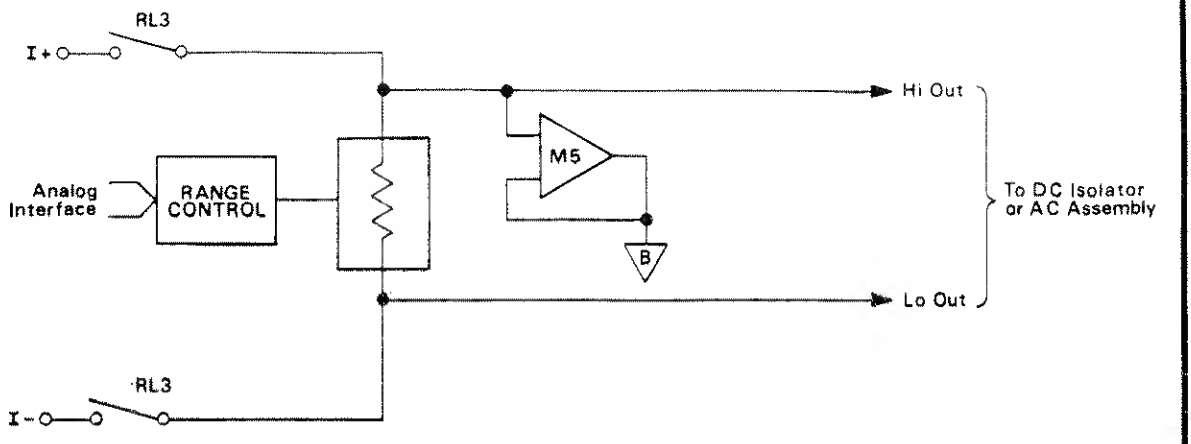


FIG. 3.32 SIMPLIFIED DIAGRAM OF CURRENT ASSEMBLY

3.5.1 Current Measurements

Precision current shunts of 0.1Ω, 1Ω, 9Ω, 90Ω and 900Ω connected in series provide an output of 100mV for a full range signal. To eliminate errors in measurement due to lead or contact resistance, all current shunts are 4-wire sensed i.e. a pair of current leads and a pair of voltage leads to the shunt(s) switched separately. The voltage developed across the shunt(s) is fed to the DC Isolator in DCI and the AC assembly in ACI or DCI + ACI. The latter, DC coupled mode, computing the RMS value of the DC and AC component of the input current. These circuits are placed in the '.1V range' amplifying the signal by 3.16. The output of buffer M5 is used to guard leakage paths on the current board.

Overload protection up to 2 amps is provided by diodes D13 – D16. An input greater than 2 amps causes the current fuse, located on the rear panel, to blow.

3.5.2 Test

During the self test routine, the Current assembly is checked for correct operation. The circuitry is placed into the .1mA DC current range as described in Section 3.2.1.3 with the DC Isolator in the 100mV range. Filter is selected and F.E.T. Q9 closed from M4 – 10 allowing current to flow through R18 to the 100μA range shunts, from the +15V supply. Thus a voltage of approximately 0.3 volts is developed across the shunts and fed to the DC Isolator. This voltage combined with the effect of the voltage injected due to the DC Isolator being in Test (Section 3.2.2.6) causes the output of the DC Isolator to be approximately 5.75 volts. After measurement by the A-D converter, the value is compared to the stored value. If the measured signal is within 6% of the stored value, the test is complete.

3.6 REAR INPUT/RATIO INPUT (Circuit Drawing No. 430307).

3.6.1 General

The Rear Input/Ratio Input assembly contains the switching circuitry to enable one of the three analog signal sources to be connected to the measurement circuits of the DVM. When Rear Input is selected either remotely or on the rear panel of the instrument and the RATIO key is depressed, the switching circuitry, under microprocessor control, selects the ratio (reference) input then the rear (signal) input, taking one valid reading at each stage.

3.6.2 Front Panel/Rear Panel Input

When Front Input is selected, either remotely or on the rear panel, this causes the base of Q1 to be connected to 0 volts, turning on the transistor. Thus relays RL1 and RL2 are energised, causing the front signal input terminals to be connected to the measurement circuits. Should Rear Input be selected, relays RL1 and RL2 are de-energised, connecting the rear input to the measurement circuits.

3.6.3 Ratio

During the last part of the analog interface update sequence (see Fig. 3.6) M1-5 is taken high causing the flip-flop (M1) to be clocked high (0 volts) on pin 1. The signal is applied to Q2 energising the ratio mode input selector relays, RL3 and RL4. Thus the inputs to the 'Ratio Input' on the rear panel are connected to the measurement circuits. Once a valid reading has taken place, the 'Rear Input' lines are connected to the measurement circuits by leaving M1-5 low. This de-energises the relays as Q2 is turned off. Another reading is then taken and the ratio calculated.

3.6.4 Test

When TEST is selected, the ratio option is checked to see if it is fitted, by interrogating the AD4 line to see if it is held high.

3.7 ANALOG OUTPUT (Circuit Drawing No. 430308)

3.7.1 General

The Analog Output 8oard accepts the DC Isolator or AC Converter Output and converts it to a ±1 volt DC full range output. This signal can then be used, for example, to drive X-Y plotters or strip chart recorders.

3.7.2 Description

The 3.16V full range signal from the DC Isolator or AC Converter is buffered by unity gain amplifier M2. The output is potentially divided by R7 and R8 so that 1 volt full range is presented to M1, another unity gain amplifier. Potentiometer R5 is adjusted to remove any offset caused by M1 and M2. Positive temperature coefficient thermistors R3, R4 and diodes D1, D2, protect the Analog Output circuitry from accidental input applied to the Analog Output external connector.

3.8 DIGITAL ASSEMBLY (Circuit Drawing No. 430329)

The Digital assembly contains the circuitry oroviding the general management of the instrument and the digital section of the A-D converter. Fig. 3.33 outlines the main portions and signal highways of this board.

3.8.1 Processor and Memory (430329 sheet 1)

A 6800 microprocessor (MPU) together with 16k bytes of memory controls the communication between the front panel, digital interface, display drivers, Digital and analog assemblies. The memory can be split into five main areas: –

(1) Program Memory - needed to operate the whole instrument system.

(2) Constant Data Memory - e.g. Self Test limits, Error read-out specifications and other fixed factors.

(3) Non-volatile Calibration Memory - used to store all the calibration errors used for each reading and determined during the 'Auto-cal' cycle.

(4) Operating Memory - used for scratch pad operations and storing.

(5) Volatile Display Memory - volatile data such as Max-Min stores, Limit stores and computation stores.

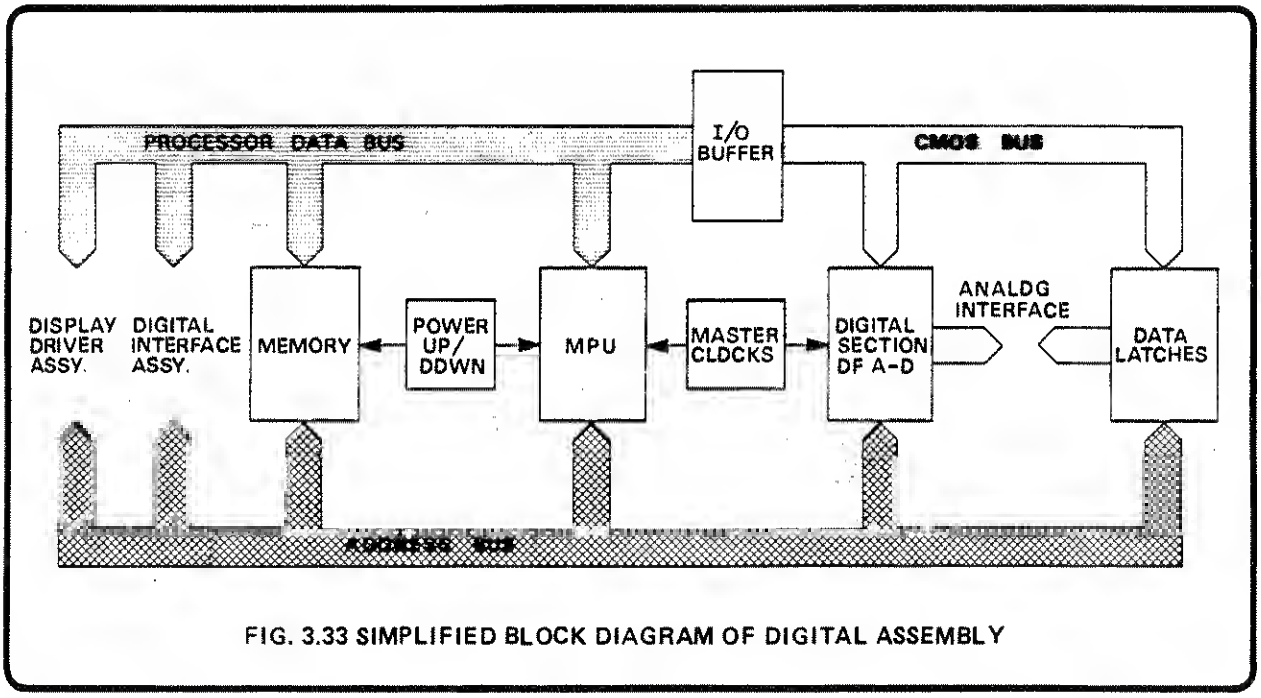


FIG. 3.33 SIMPLIFIED BLOCK DIAGRAM OF DIGITAL ASSEMBLY

3.8.1.1 Software Overview

The system uses the technique of a looping prioritised job scheduler (see Fig. 3.34). Each job driven from the scheduler is controlled by a flag in the system workspace which is set when the job is required to be run and cleared when completed. Priority of activation is ensured by making each job exit on completion, to the top of the schedule.

Program Modules: The program memory is split into a series of functional modules, each module corresponding fairly closely to a major functional area and hence to one of the jobs activated by the job scheduler, the larger ones being sub-divided, see Drawing No. 890043.

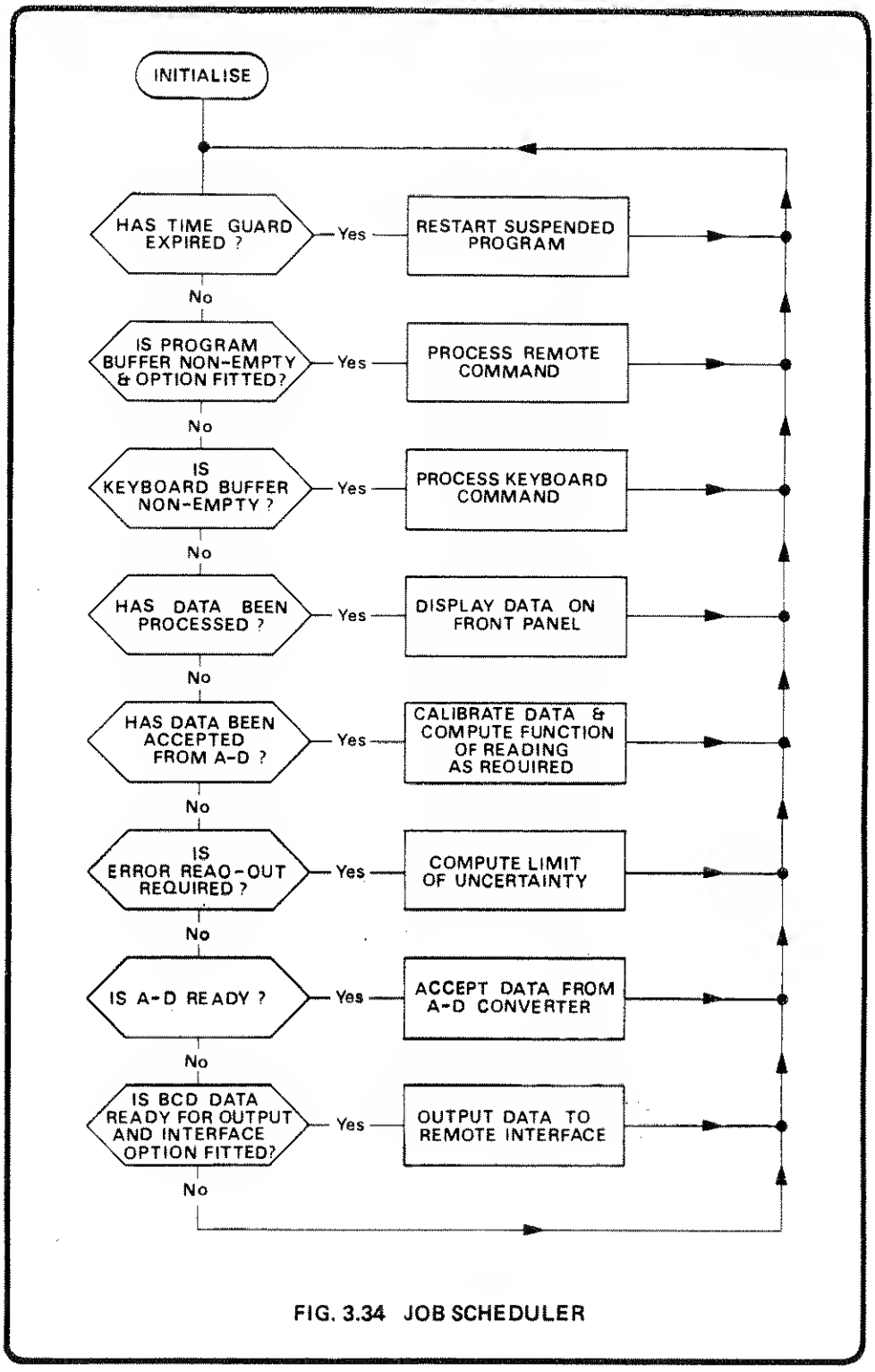


FIG. 3.34 JOB SCHEDULER

3.8.3 Analog to Digital Conversion (Digital Section)

3.8.3.1 General Principle

Block diagram Fig. 3.40 outlines the essentials of the digital section and should be used with flowchart Fig. 3.41 in order to follow the operation of this section.

The function of this section of the circuitry is to generate the sequence that when transferred to the analog section, controls the sequence from RESET through the integration cycle and beck to RESET. The circuitry controls the length of SIG and BIAS and counts during REF 1 and REF 2, the accumulated count being proportional to the length of the reference periods, which in turn is proportional to the measured input signal. At the end of each reading cycle the count is read by the MPU, processed and displayed.

The sequence is controlled by stepping M47 through Q0 to Q7. Each 'Q' output from M47 goes to logic-1 to activate its stage of the sequence; completion of one stage generates the 'Enable' for the next, via M46 switches, as a logic-0 state at M47-13. Timing is synchronized by Master-Clock/2 positive-going edges at M47-14, when M47 is enabled.

3.8.3.2 Preset Procedure

As part of the initialisation routine (at switch on), M47 (used as the sequence controller), is reset from M37-11, causing M47-2 to be logic '1'. Thus the control lines $\overline{A}$, $\overline{B}$ and $\overline{C}$ put the analog section of the A-D into RESET (See Fig. 3.42). The Address Bus decoded signal XADDLY is taken low, enabling the presetting of the delay counters M13 and M14 from the CMOS Data Bus, the amount of delay being determined by the selected range, function and filter state, see Fig. 3.43. The A-D control latches, M11 and M12 are then enabled by XADCTL to (i) reset the command latch M1 (from M11-4), (ii) set the resolution of the main counter (M11-5 and 6), (iii) select trigger gate (M12-3, 4 or 5) and (iv) reset the data ready latch (M12-6).

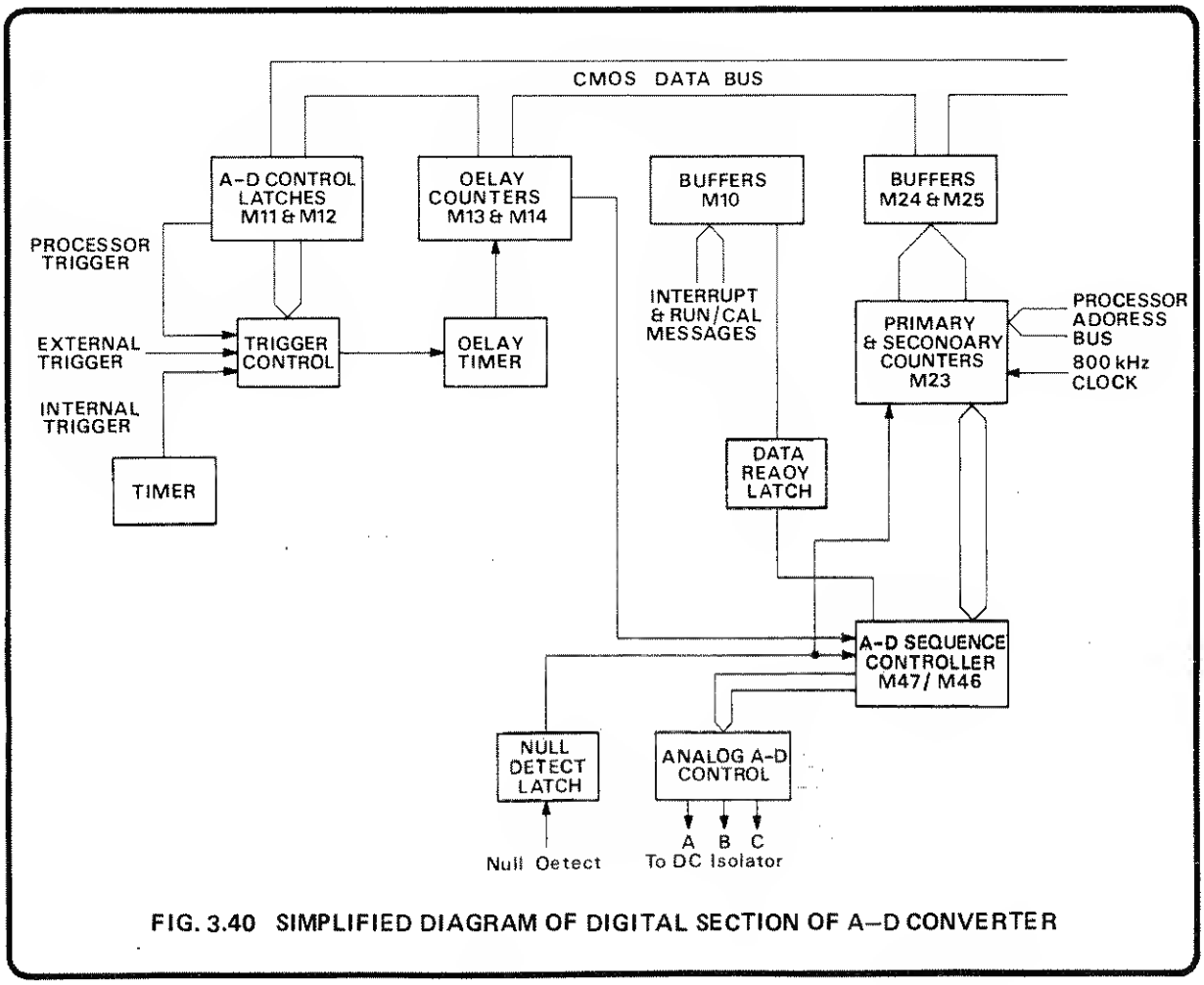


FIG. 3.40 SIMPLIFIED DIAGRAM OF DIGITAL SECTION OF A–D CONVERTER

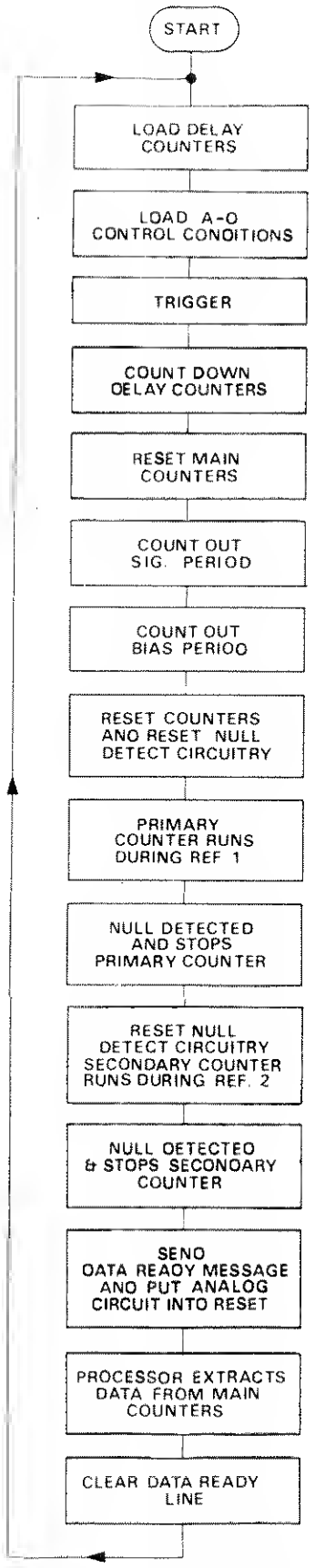


FIG. 3.41 FLOWCHART OF A–D DIGITAL SECTION

SIGNAL	$\bar{A}$	$\bar{B}$	C
RESET	1	1	0
SYNC	1	1	0
SIG	1	1	1
BIAS	0	1	1
WAIT	0	1	1
REF 1	1	0	1
REF 2	0	0	1
END	1	1	1

FIG. 3.42 A-D ANALOG SEQUENCE CONTROL SIGNALS

1061/A SELECTIONS		M13/M14 COUNT	
FUNCTION	RANGE	$\overline{\text{FILTER}}$	FILTER
DCV	All Ranges	2	101
Option 12 ACV DCV + ACV	All Ranges	61	251
Option 10 ACV DCV + ACV ACI DCI + ACI	All Ranges	46	151
DCI	100μA-1mA	2	
	10mA	3	101
	100mA	5	
	1A	6	
kOhms	10Ω-100kΩ	2	101
	1MΩ	4	121
	10MΩ	31	251

FIG. 3.43 COMMAND DELAYS

3.8.3.3 A-D Measurement Sequence

Trigger. The trigger, required to initiate the measurement sequence, is generated from one of three possible sources:

1. Internally generated 3/second trigger, from timer M61-7.

2. Externally generated trigger, from EXT TRIG on rear panel via M24-13.

3. A MPU derived trigger from M11-3 generated when auto-ranging, pressing MANUAL when HOLD selected, during calibration, an INPUT ZERO sequence or via the digital interfaca.

The trigger source is selected by the latched data on M12, enabling one of the three gates of M2.

Delay. The trigger pulse clocks the 'command latch' M1-11 causing the timer, M15, to output clock pulses (200Hz) to the delay counters (M13 and M14) after a delay of approx. 1.5mS set by C5, R8, R9, R11. The delay counters proceed to count down to zero, at which time the delay latch (M26) is clocked. Thus M26-14 becomes a logic '0', enabling the sequencer M47 (an octal counter) to proceed on to the next step via M46-2.

SYNC. The SYNC phase from the sequencer resets the counters of M23 and places the analog section of the A-D into SIG. The pulse is fed back to M47 via M46-3 to step on the sequencer.

SIG. During the time that the SIG line is at logic-1 (M47-3), the primary counter in M23 is enabled and counts out the signal period (20ms in normal mode, or 2.5ms superfast). When the counter times out, M23-23 goes to logic-0, enabling M47-13 via M23-14. The next Master-Clock/2 at M47-14 steps the sequence on to BIAS (M47-7 to logic-1, M47-3 reverts to logic-0).

BIAS. The BIAS signal (M47-7) is transferred to the analog section of the A-D by changing the state of the $\overline{A}$ line (M38-9 to a logic '0'). BIAS also enables the secondary counter of M23 to count out the BIAS period (20μS). The signal indicating the end of this period is passed via M46-9 causing the sequencer to carry on to the next step. The BIAS signal also resets the 'delay latch' (M26) ready for the next measurement cycle, and the 'null detector' latch (M22A).

WAIT. The WAIT pulse resets the counter of M23 via M39-10, keeps the $\overline{A}$ line to the analog section low, clocks the polarity null detect latch M22(B) causing a logic '1' on pin 1 if the signal applied to the analog section of the A-D converter was positive (logic '0' if negative) and is fed back to enable the sequencer via M46-3.

REF 1. The high to low edge of WAIT causes the $\overline{A}$ to change state and going into REF 1 makes $\overline{B}$ a logic '0'. The analog side is then in the condition to start 'ramping down'. While REF 1 is high the primary counter of M23 is enabled (pin 3) and counts the period of REF 1.

REF 1 is ended when a null detector pulse is detected and latched on to M22. This causes the sequencer to step on once more from M46-3, the low to high edge from pin 4 disabling the primary counter.

REF 2. The REF 2 signal changes the state of the $\overline{A}$ line (causing the analog section to ramp down at a slower rate), resets the 'null detect' latch and enables the secondary counter of M23 (Pin 13) to count the period of REF 2. If the secondary counter overflows, the primary counter is incremented from M23-16.

As in REF 1, a null detector pulse causes tha counting period to end (M22-12) and increments the sequencer via M46-3 causing the $\overline{A}$ and $\overline{B}$ lines to change state.

END. The low to high edge from M47-10 is fed back to M47, via M48-6 giving a master reset. Thus the sequencer is placed into RESET.

RESET. The sequence pulse from M47-2 clocks the 'data ready' latch M1-3 placing a signal on to the CMOS Data Bus via tri-state buffer M10 indicating to the MPU that a reading is ready to be taken from the main counter M23. Data is extracted from the counters in three bytes (controlled by the A1 and A0 lines of the processor address bus) with the counter output buffers, M24 and M25 being enabled by $\overline{XADDT}$, a decoded processor address.

The RESET signal is also passed to the analog section of the A-D by changing the state of the C line.

Once the data has been extracted from the main counter the set-up procedure is then repeated to await a further trigger.

3.8.3.4 **Master Clock and Line Locking (430329 sheet 4)**

To give improved rejection of line frequency related noise, the 1061 is linelocked. The line frequency is sampled and compared to the internal master clock. Synchronisation is achieved by adjusting the master clock frequency.

A sinusoidal line frequency signal from the 5V mains tap is convertad to a square-wave (M25-13) and ÷2(M26-1) before being fed to the comparator section of the ULA M23 (sheet 3). The MASTER CLOCK ÷2 signal is fed to ripple counter M27 which outputs a signal of twice the estimated line frequency, for line related periods, controlled by the ULA (M23-18). This signal is fed to M23-19 (via inverter M39) and after a further ÷2, is compared with the actual line frequency (see Fig 3.44).

The ULA determines whether the master clock is running too slow or too fast, producing a signal on pin 20 whose pulse-width is proportional to the difference. The output of pin 21 is a 25Hz square-wave which is fed to the up/down input of counters M41/50. Thus depending on the position and down period of the pulse, the count held is increased or decreased.

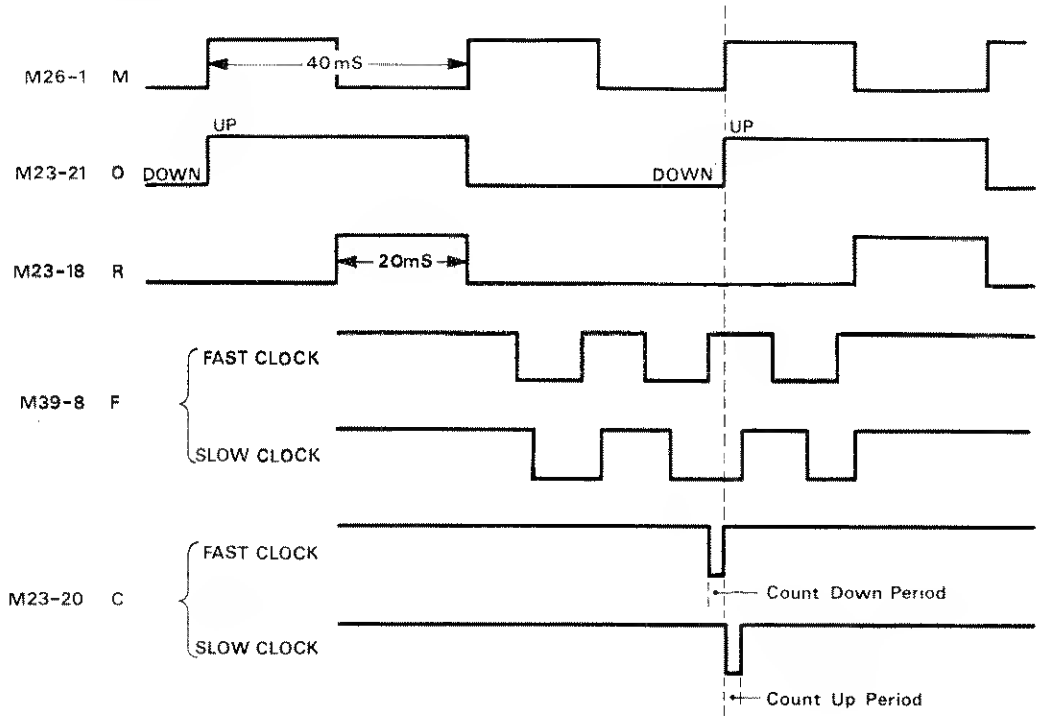


FIG. 3.44 LINE LOCKING TIMING DIAGRAM (50Hz)

Latches M42/51 are updated with this new count during the A-D RESET period and applies the count to resistor network AN4 which forms a D-A converter. Changing the voltage applied to varicap D9 alters its capacitance, thus adjusting the LC of the Colpitts oscillator. Therefore the frequency of the Master Clock is increased or decreased to be an exact multiple of the mains frequency.

3.9 FRONT PCB ASSEMBLY (Circuit Drawing No. 430294)

The Front pcb assembly accepts the measurement signals, digitally displays the value, provides manual control of the measurement circuits and data conditioning, and gives a visual status indication of the selectable instrument states.

3.9.1 Analog Input Signals (430294 sheet 2)

The Front pcb connects the terminals to the 2/4-wire Ohms and Local-Remote Guard switches. Thus in '2-wire': Hi is connected to I+, and Lo to I−, through thermistors R1 and R2. In 'Local': Guard is not directly linked to the front panel Lo terminal, as this becomes active in 4-wire Ohms. Instead, 'Local' links Guard to Ohms Guard, which is permanently connected to DC Isolator Lo.

Signals applied to the six front panel terminals are routed through to the Rear pcb (to the Rear Input/Ratio pcb or Rear Input pcb if Option 40 or 41 is fitted) via the Signal Cable assembly. Each of the terminal leads passes through its own HF choke, all six inductors being wound in the same direction on the same core. This 'Common Mode' choke presents high impedance to transient common mode currents, but low impedance to normal mode differential input currents.

Two screened cables are used to transfer the signals to the rear: I+ and Hi are carried in one; I−, Lo and Ohms Guard in the other. Guard is carried via the cable screens, thus guarding the signals during transfer.

3.9.2 Display Signals (430294 sheet 1)

The front panel assembly routes the display signals from the Display Driver board to the gas discharge display.

3.9.3 Keyboard Data Encode (430294 sheet 1)

Selection of a front panel keyswitch causes one of the two 16-key encoders (M7 or M10) to send a data available message to M2 (a data latch) and to remember which key was pressed. The output of M2, (pin 1 or 13) signals the interrupt circuitry of the Digital Board (IROK1 or IROK2).

When the microprocessor accepts the interrupt and has located the source, the XKY BRD line to pin 13 of M7 and M10 is taken low, enabling the data outputs of the encoders to be placed on to the CMOS data bus (See Fig. 3.45 for the key select coding). This signal also resets M2 ready for the next key selection.

KEY	M7			
	14	15	16	17
	CD7	CD6	CD5	CD4
100	0	0	0	0
10	0	0	0	1
1000	0	0	1	0
10MΩ	0	0	1	1
1	0	1	0	0
.1	0	1	0	1
10Ω	0	1	1	0
AUTO	0	1	1	1
DC	1	0	0	0
kΩ	1	0	0	1
KEYBOARD	1	1	0	1
I	1	1	1	0
INPUT ZERO	1	1	1	1

KEY	M10			
	14	15	16	17
	CD3	CD2	CD1	CD0
HOLD	0	0	0	0
RATIO	0	0	0	1
TEST	0	0	1	0
SPEC	0	0	1	1
(A–B)	0	1	0	0
dB	0	1	0	1
÷ C	0	1	1	0
MAX	0	1	1	1
MIN	1	0	0	0
RESET	1	0	0	1
MAN	1	0	1	0
INPUT FILTER	1	1	0	1
AC	1	1	1	1

FIG. 3.45 CMOS DATA BUS : KEY SELECT CODING

3.9.4 Keyboard L.E.D. Data Decode (430294 sheet 1)

The XKY 8RD signal is inverted by O1, R7, C1, R6 partially enabling the L.E.D. data latches M4, M5, M6, M8, M9, M11 and M12 while information is not being extracted from the keyboard encoders. The data latches are divided into four sets, M6 and M4, M8 and M5, M12 and M11, M9 being fully enabled from the XKD SPØ – XKD SP3 lines respectively.

On initialisation or after a change of the instrument's selectable states, the L.E.D. data latches are updated by placing data on the CMOS Data Bus (See Fig. 3.46), firstly to M8 and M5 (enabled from XKD SP1) and 'clocking' from the CMOS CLK line (J2-6), secondly to M12 and M11, then M9 and finally M6 and M4.

The output of the L.E.D. latches provide the signals to the bases of the L.E.D. drive transistors, switching them on or off as required.

CMOS DATA LINE	M12/M11	M8/M5	M6/M4	M9
CDO	÷C	DC	AUTO	
CD1	dB	kΩ	10Ω	
CD2	SPEC	INPUT ZERO	.1	
CD3	TEST	INPUT FILTER	1	
CD4	A–8	KEYBOARD	10	
CD5	MIN		100	MAN
CD6	MAX	I	1000	RATIO
CD7	RESET	AC	10MΩ	HOLD

FIG. 3.46 CMOS DATA BUS : LED-SELECT CODING

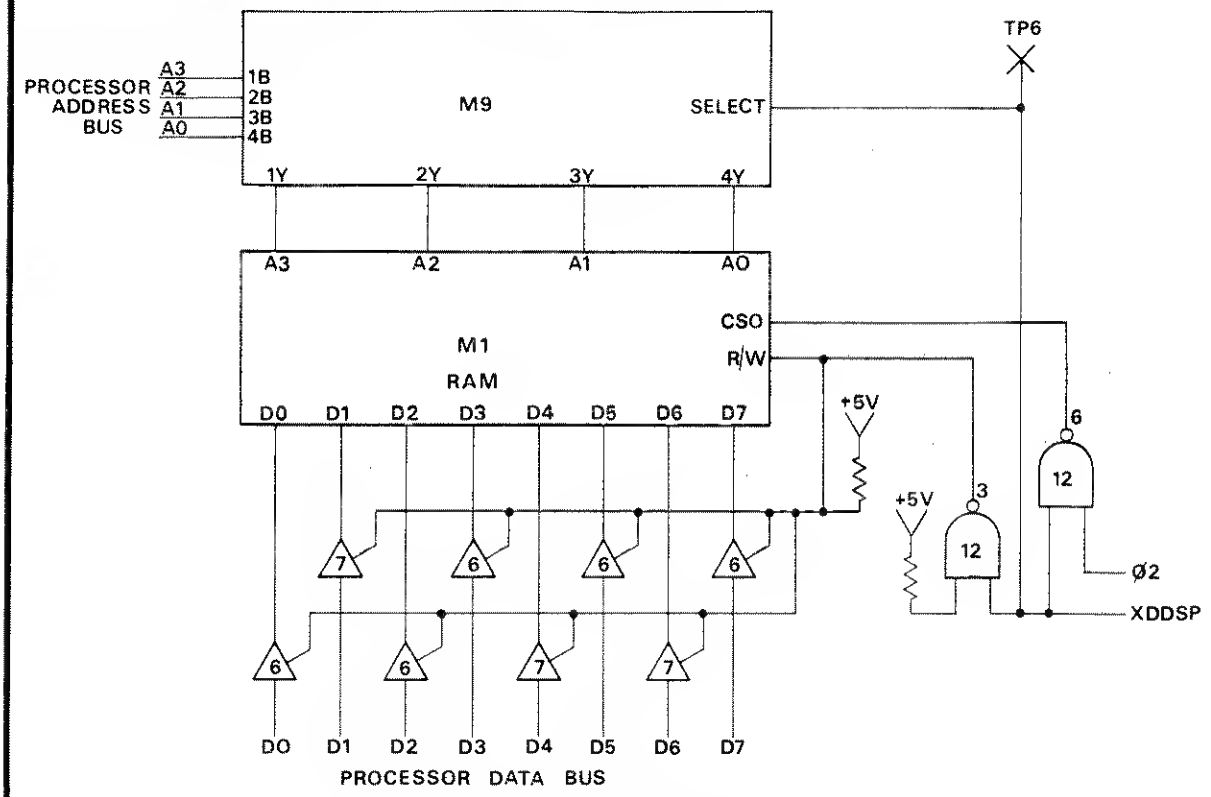


FIG. 3.47 DISPLAY DRIVER WRITE CIRCUITRY

COUNTER (M8)				RAM (M1)				Display block energised or operation implemented from M11
Q_3	Q_2	Q_1	Q_0	A_3	A_2	A_1	A_0	
0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0	3
0	0	1	0	0	1	0	0	5
0	0	1	1	0	1	1	0	7
0	1	0	0	1	0	0	0	9
0	1	0	1	1	0	1	0	11
0	1	1	0	1	1	0	0	
0	1	1	1	1	1	1	0	
1	0	0	0	0	0	0	1	2
1	0	0	1	0	0	1	1	4
1	0	1	0	0	1	0	1	8
1	0	1	1	0	1	1	1	8
1	1	0	0	1	0	0	1	10
1	1	0	1	1	0	1	1	Reset Counter

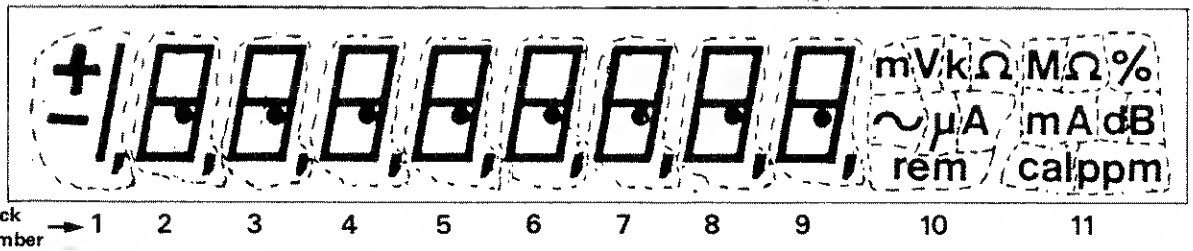


FIG. 3.48 DISPLAY DRIVER READ MODE ADDRESS STATES

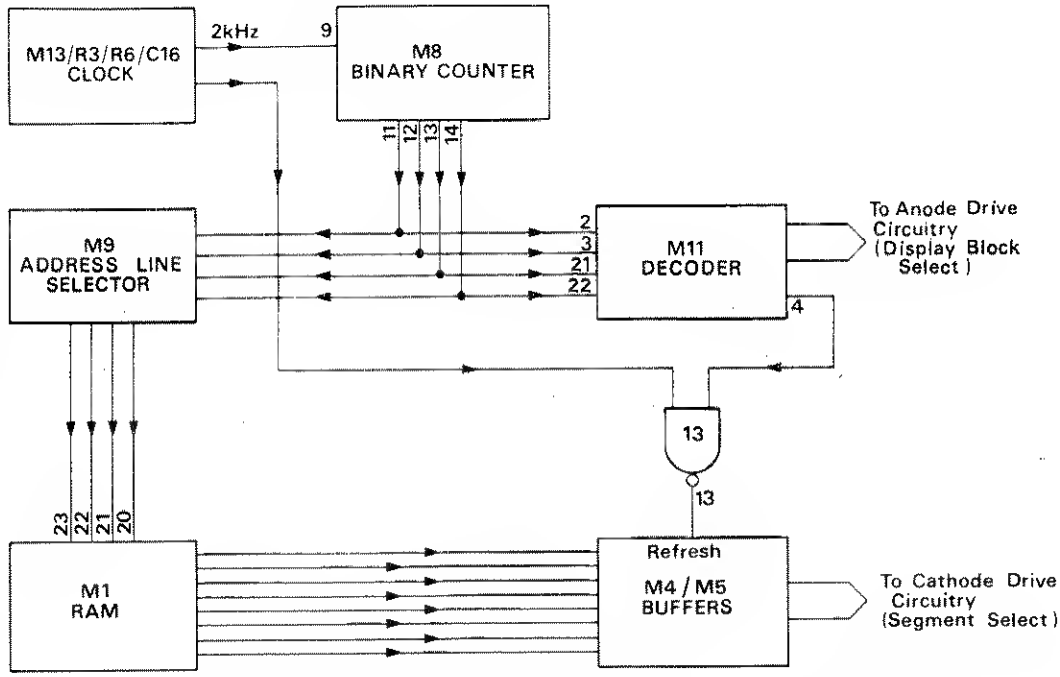


FIG. 3.49 SIMPLIFIED DISPLAY DRIVER READ CIRCUITRY

3.10 DISPLAY DRIVER ASSEMBLY (Circuit Drawing No. 430330).

Basically, the Display Driver assembly receives the display information from the microprocessor (running at 800kHz) and stores it in a Random Access Memory (RAM) digit by digit. This data is then read out at a slower frequency (2kHz), level shifted and output to the gas discharge display.

NOTE: In the following description, each bar, decimal point or legend is referred to as a display segment and each set of segments i.e. ±1, ⊟ or a legend block, is referred to as a display block.

3.10.1 Write Mode

On completion of a reading or when certain modes are selected, (e.g. ERROR, keyboard entry), the processor indicates to the Display Driver Board that data is ready to be transferred by the signal XDDSP (TP6). This causes the RAM (M1) to be placed into its write mode and the quadruple 2-line to 1-line data selector, M9, to select the '8' inputs which are connected to the processor address bus.

The signal XDDSP also causes the tri-state buffers M6 and M7 to become enabled, causing the data input lines of the RAM to be connected to the processor data bus. Thus under MPU control, the display data (±1, ⊟ 's, decimal points and legends) is written into the RAM.

Once this transfer of data is complete the RAM becomes deselected, the buffers return to their third state inhibiting the data bus to the RAM and connects the 'A' inputs of M9 to the address lines of the RAM.

3.10.2 Read Mode

Discharge between adjacent display blocks is prevented by time multiplexing and sending information to alternate blocks. A particular display block is selected by driving its anode, and a particular segment by driving the segment cathode.

The free running clock M13, R3, R5, C16, produces a 2kHz signal (M13-9) to drive a 4-bit binary counter, M8, which provides the control of the address lines in the read mode (See Fig. 3.49). The display block selection is achieved by decoding these 4 lines into 16 bits using M11. The output lines of M11 are connected to the bases of transistors Q1-Q3, Q13-Q20 which act as anode switches. Note that when the address lines are in the state 0000 the output of M11 (pin 11) selects the anode to block 1, 0001 selects the anode to block 3 (M11-9), 0010 ... block 5, etc., thus the display blocks are selected alternately.

To select the appropriate segment data from the RAM to match the display block selection the address lines are given a left hand bit rotation, i.e. if the output of M8 is labelled DC8A, (2^3, 2^2, 2^1, 2^0), the address input of M1 would be C8AD. (Fig. 3.48 gives the state of the address lines for each display block). The particular display block segment data is recalled by the RAM, buffered by M4 and M5, level shifted -180 volts by R8-R15, C4-C11 causing Q5-Q12 to drive the cathodes, D1-D10 acting as restoration diodes. Between the transfer of each set of segment data, M13-13 is taken high, causing the outputs of M4 and M5 to be a logic '0'. This produces a refresh period for capacitors C4-C11 to discharge from the -180V supply through the restoration diodes.

3.11 IEEE 488 STANDARD DIGITAL INTERFACE (Circuit Diagram No. 430427)

The IEEE Digital Interface assembly contains the extra memory circuitry required for the execution and decoding of interface functions, and for data input and output transfers. Simplified diagram Fig. 3.50 shows its essential features.

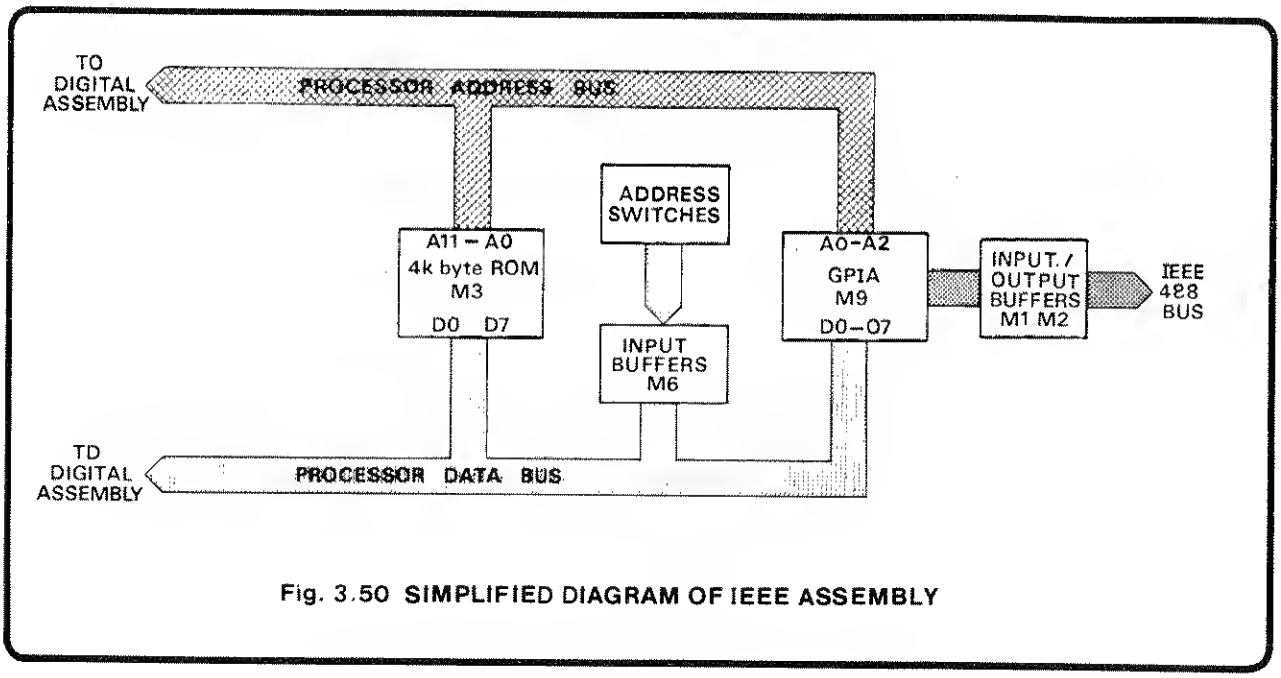


Fig. 3.50 SIMPLIFIED DIAGRAM OF IEEE ASSEMBLY

3.11.1 ROM Circuit

The IEEE Digital Interface assembly acts as an extension to the Digital assembly with connections to both the Processor Address and Data 8uses. The board houses 4k bytes of program memory (M3) containing the sub-routines to control the instrument from the IEEE 488 Bus. The ROM receives the address information, with chip selection being made by decoding address lines A3-A11 with XIOBD and master clock Ø2.

3.11.2 Interface Circuit

The General Purpose Interface Adaptor (GPIA). M9, provides the interface between the IEEE 488 Standard Instrument 8us and the 68000 microprocessor. The MPU can receive, process and send messages to the interface through the GPIA.

The GPIA is able to automatically handle the following interface protocal[1] :-

Single address capability
Source and acceptor handshake
Talker and Listener states
Service Request
Parallel Poll
Device Clear
Device Trigger

With MPU it is also capable of:-
Programmable Interrupts
Storing the instrument's address
Control of the interface input/output buffers.

The GPIA is selected by decoding address lines A3-A11 with XIO8D. Address lines A0-A2 with the state of the MPU R/$\overline{W}$ line select one of the 8 read only or 7 write-only registers in the GPIA, enabling the MPU to send or receive data over the interface.

The two signals T/$\overline{R}$1 and T/$\overline{R}$2 are used to control low power transceivers (formed from M1, 2) which drive the interface bus.

[1] For further information refer to 'Getting aboard the 488 Bus' published by Motorola.

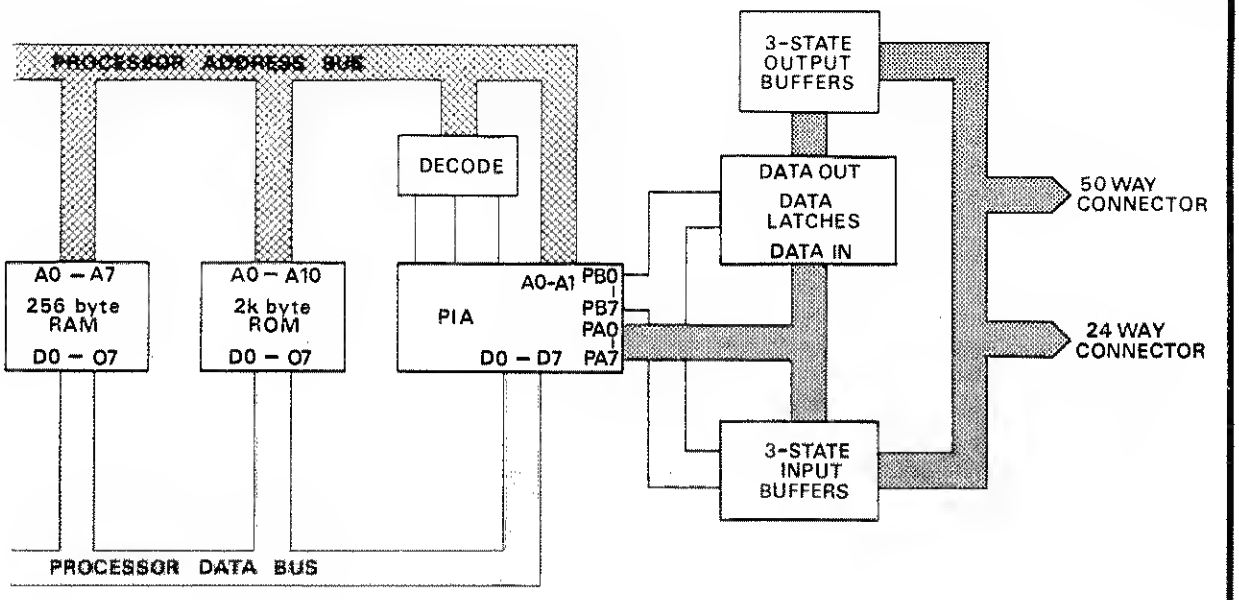


FIG. 3.51 SIMPLIFIED DIAGRAM DF BCD INTERFACE ASSEMBLY

3.12 BCD DIGITAL INTERFACE (Circuit Drawing No 430332)

The BCD Digital Interface assembly contains the extra memory and circuitry required for the execution and decoding of interface functions and to perform data output transfers. Simplified diagram, Fig 3.51 shows the essential features of this board.

3.12.1 RAM/RDM Circuit

The BCD Digital Interface assembly acts as an extension to the Digital assembly with connections to both the Processor Address and Data Buses. The board contains 2k bytes of program memory (M11) containing the sub-routines to control the instrument from the BCD Interface. Extra 'operating (scratch pad) memory' is provided by two 256x4 bit RAMS (M22, M23). Both the ROM and RAM's receive the address information, with chip selection being made by decoding address lines AB-A11 with XIOBD, R/$\overline{W}$ and Ø2.

3.12.2 Interface Circuit

The Peripheral Interface Adapter (PIA), M1, provides the means of interfacing the BCD input/output to the 6800 microprocessor. The PIA is selected by decoding address lines A9-A11 with XIOBD. Address lines A0 and A1 together with MPU data messages configure the six internal registers controlling data flow and external control signals.

Peripheral Data lines PBO-PB7 (M1 pins 10-17) are used as enable lines allowing data to be placed on the BCD Data Bus from the Remote Programming Input and control lines of the BCD Output (2 bytes) and allowing data to be placed into output latches M7-M10, M12-M16 (5 bytes).

The length of PRINT COMMAND is controlled by the timer M2, R1, C3.

3.13 REAR (POWER SUPPLY) PCB ASSEMBLY (Circuit Drawing No. 430295)

3.13.1 General

The line transformer and power supply components are situated at the rear right hand side of the instrument, when viewed from the front. Transformers T1 and T2 are of toroidal construction mounted one on top of the other and bolted to the rear panel. T1 has a split primary comprising two 115V windings, intended for either series or parallel connection depending on the line voltage. An earth screen is interposed between primary and secondary windings to minimise electrostatic coupling, and is grounded to line earth. The second transformer T2 is driven from T1. It also possesses an electrostatic screen, this time being connected to Guard.

3.13.2 180V Supply

The 180V supply is required for the gas discharge display. Bridge rectifier W1 and C6 convert the 200V AC from the secondary of T1, to DC. R6, D3, R4 and Q2 act as a constant current source being regulated by D4, R5 and Q1. The +5V line (TP2) is connected to the digital +5V line (TP3) on the Display Driver assembly.

3.13.3 5V Supply

All the logic circuitry to the right of the central printed circuit board is powered from the supply generated from the two 8.8 volt 750mA secondary windings on transformer T1. The centre tap (digital common) is linked directly to line ground via LK6. The output of rectifying diodes D1 and D2 is smoothed by C7 and C8 before being fed to regulator M1. This regulator is capable of 1 amp output and has foldback current limiting and thermal shut-down, to provide short circuit protection.

3.13.4 ±15V Supply

The output of the third secondary winding of transformer T1 (10V AC) is input to the primary of T2. The two 19.25V outputs are connected in series, with the centre tap connected to analog common. The output of bridge rectifier W2 is fed to voltage regulators M2 and M3 (wired in series), to produce positive and negative 15 volt supplies to power the analog circuitry. These regulators also include foldback current limiting and thermal shut-down, to provide short-circuit protection.

3.14 SELF TEST SEQUENCE

Selection of the TEST key places the instrument into a test routine, checking the display and basic measuring circuits. A flowchart for the routine is given in Fig. 3.53. The analog circuitry conditions for each test are given in the last subsection of the circuit description for the particular board, and the range 'F.E.T.' patterns in Appendix I-8.

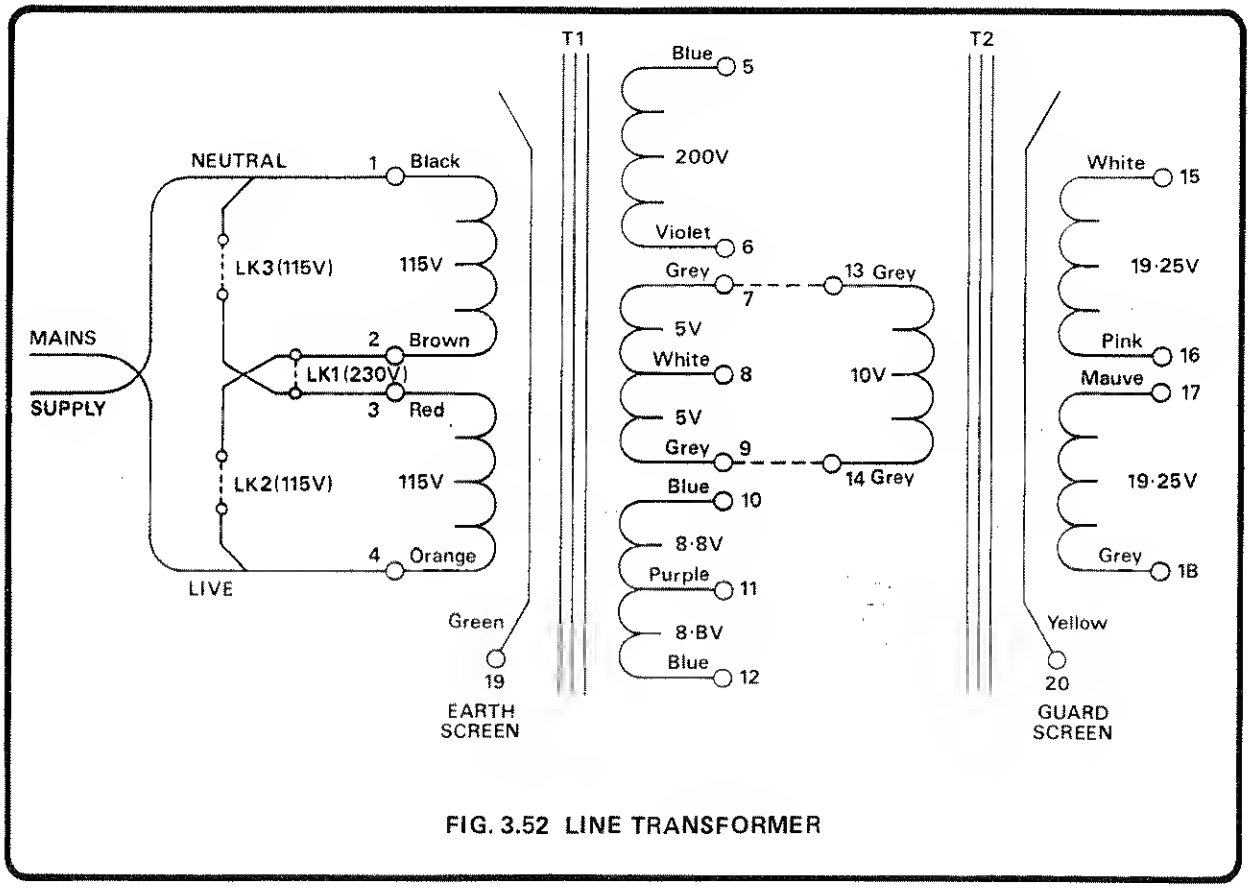


FIG. 3.52 LINE TRANSFORMER